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GAO BTX (Version: A00)

CPU: Intel Conroe, Wolfdale processors in LGA775 Package.

Notice that Apart from PRD Requirement CPU will support Yorkfield as well.

System Chipset:

North Bridge ... Eaglelake-Q43-A3
South Bridge ... ICH10D-B0

Main Memory:

Dual Channel / DDR-II * 4 (Maximum to 8GB)

On Board Device:

Clock Generator ... IDTCV184-2BPAG
Super I/O ... SMSC5524/5514E
LAN ... Boazman 82567-B0
HDA Codec ... AD1984A-04
BIOS ... SPI Flash ROM-32M

Expansion Slots:

PCI EXPRESS 16X SLOT *1
PCI EXPRESS 1X SLOT * 1
PCI SLOT * 2

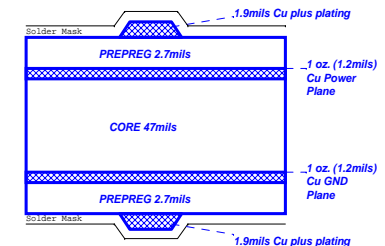
PWM Controller:

Controller ... ADP3293 (3Phase)
Driver ... ADP3120AJRZ

POP1	Proto Build	XDP, LPC HDR, SPI Debug
POP3	SIO SMSC 5524C	
POP4	SIO SMSC 5514E	
POP5	TPM STMicro(4.4mm)	
POP6	TPM Z(6.1mm)	
POP7	TPM J(6.1mm)	
POP8	TPM Winbond(4.4mm)	
POP9	QFN	

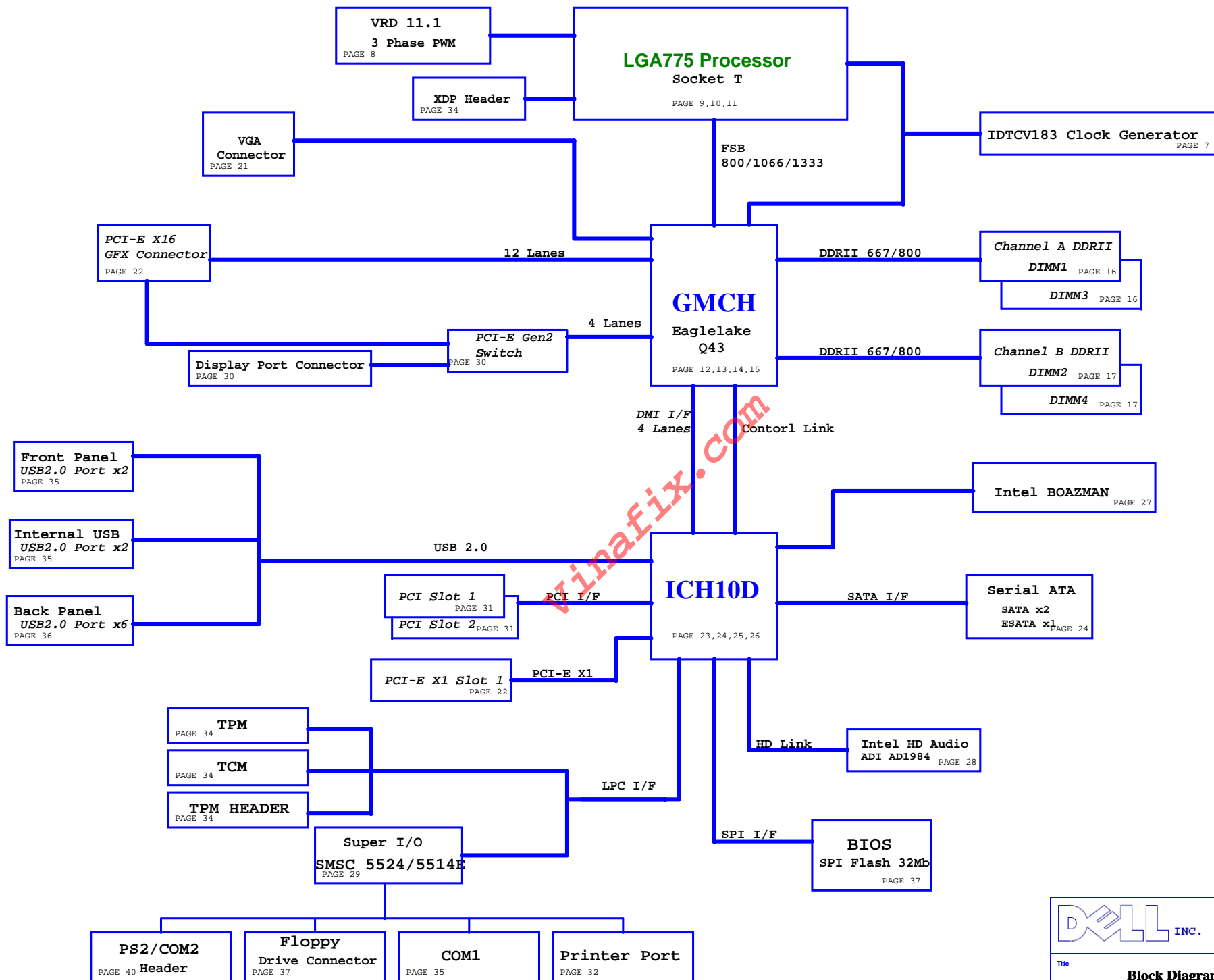
Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
PCIE - 85ohm : 15/4/8/4/15
DMI - 95ohm : 15/4/8/4/15
LAN - 95ohm : 15/4/8/4/15

DELL INC.	
Title Cover Sheet	
DWG NO GAO	Rev A00
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14.318MHz

CPU

CPU 200/266/333 MHz Diff Pair

MCH 200/266/333 MHz Diff Pair

PCI Express 100 MHz Diff Pair

PCI Express x16 Gfx

DOT 96 MHz Diff Pair

PCI Express/DMI 100 MHz Diff Pair

PCI Express/DMI 100 MHz Diff Pair

USB/SIO 48 MHz

ICH 33 MHz

REF 14 MHz

CK PCI STOP

CK CPU STOP

PCI 33 MHz

PCI Slot 1

PCI 33 MHz

PCI Slot 2

TPM 33 MHz

TPM 1.2

Boazman LAN

SIO 33 MHz

SATA 100 MHz Diff Pair

PCI Express 100 Mhz Diff Pair

PCI Express 100 Mhz Diff Pair

PCI Express x1 Slot

XDP 100MHz Diff Pair

XDP

DDRII 4 Slots 12 Diff CLKs

Channel A DDRII DDRII 667/800

DIMM1

DIMM2

Channel B DDRII DDRII 667/800

DIMM3

DIMM4

GMCH
Eaglelake

ICH10

Azalia Bit Clock

32.768KHz

Super I/O

HD Audio

IDT CV184 ClockGen



Title

Clock Distribution

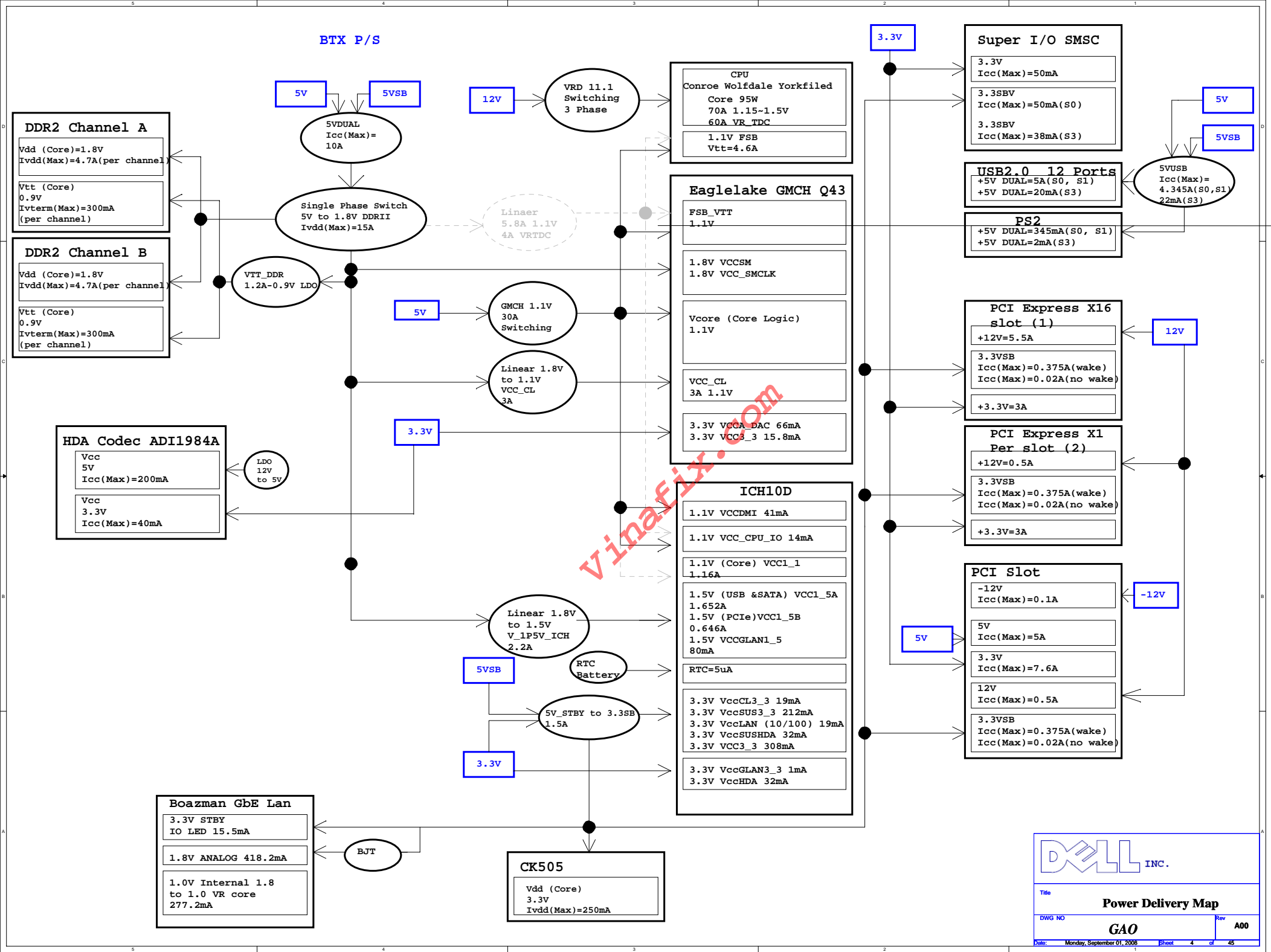
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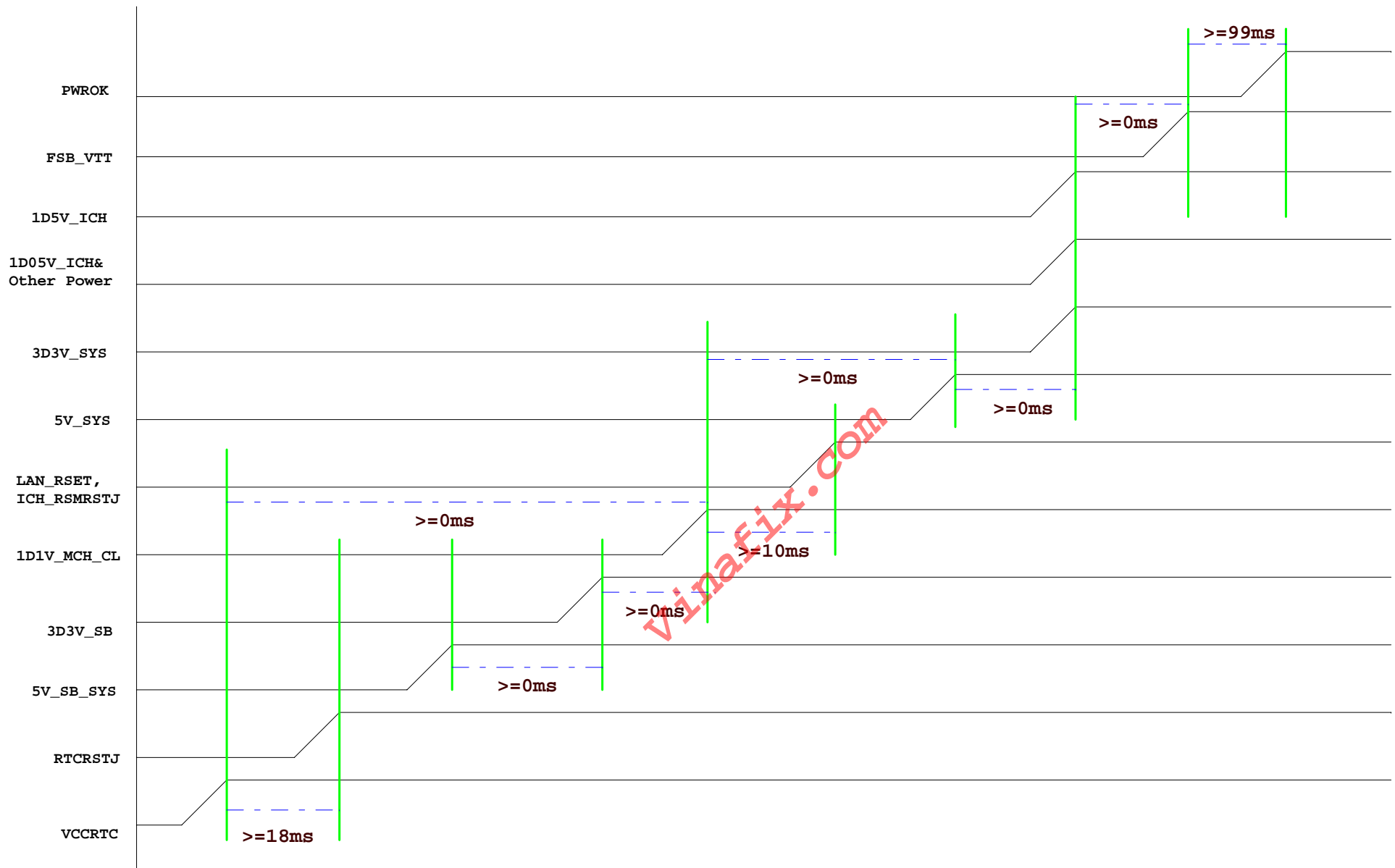
GAO

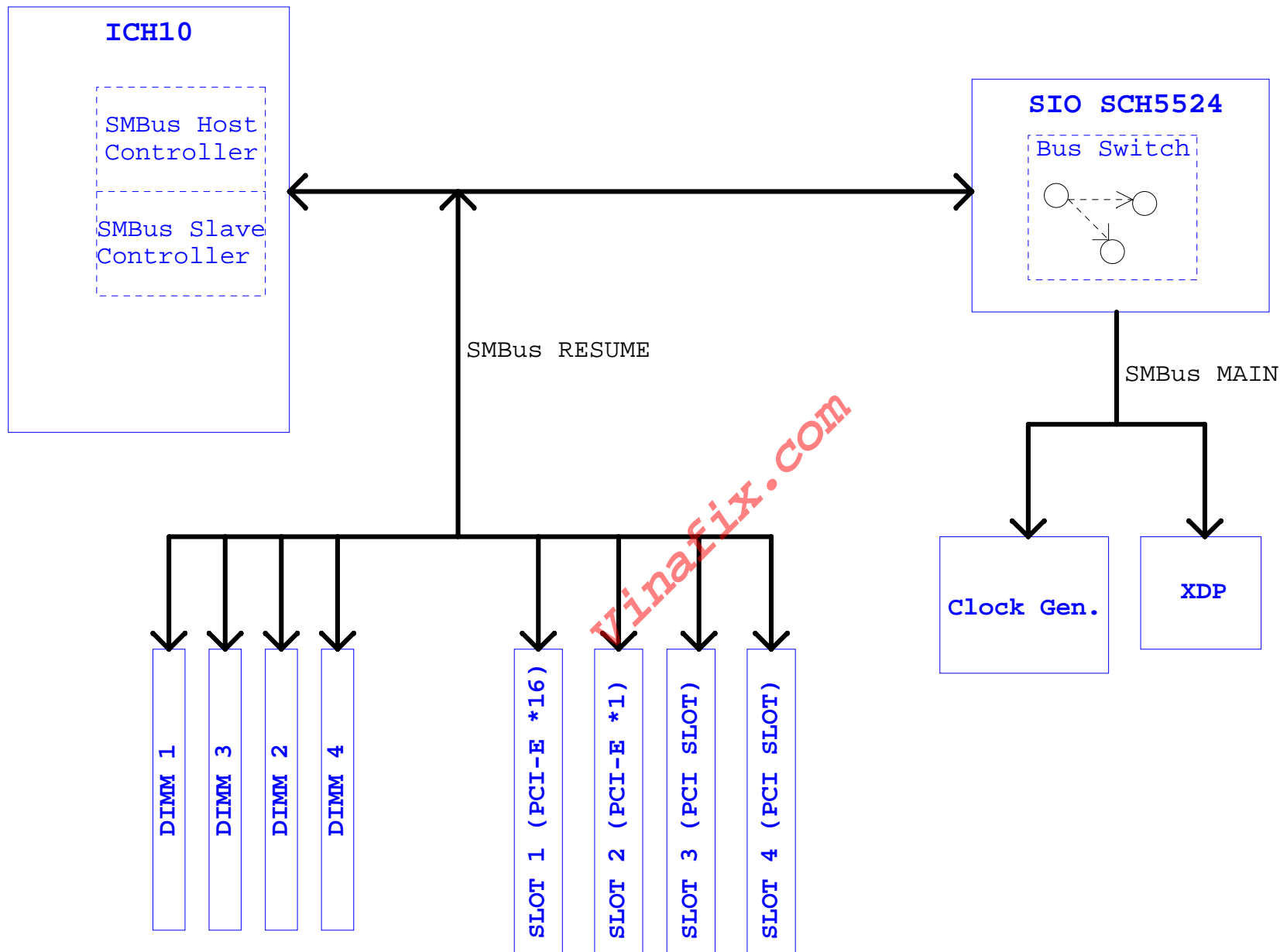
Rev
A00

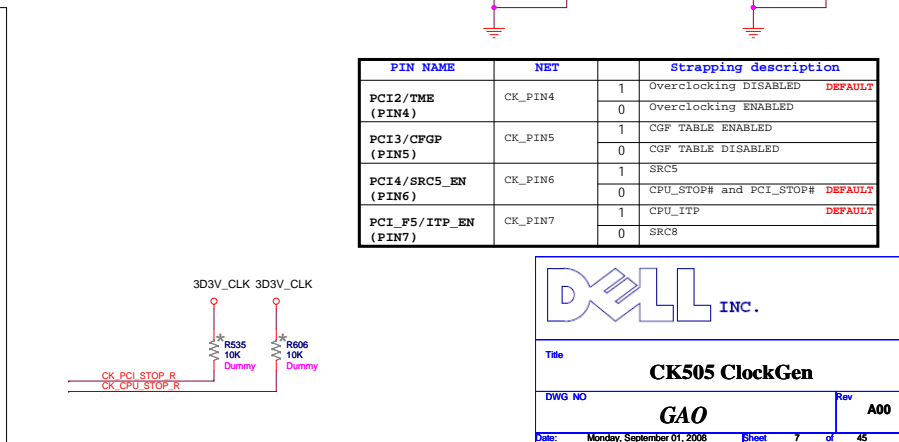
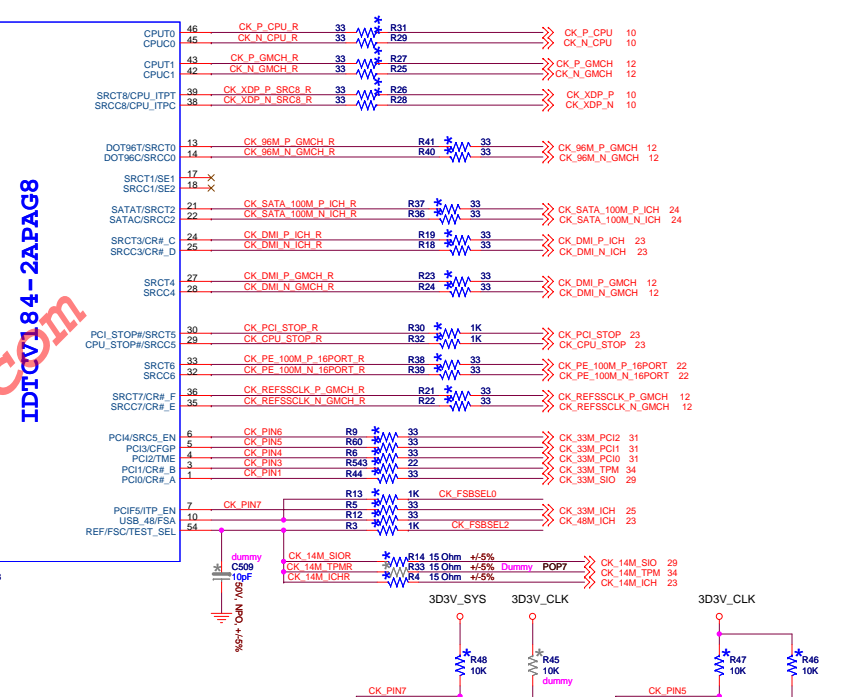
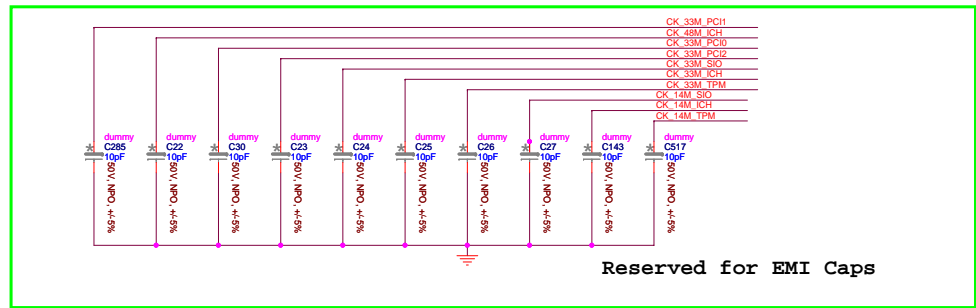
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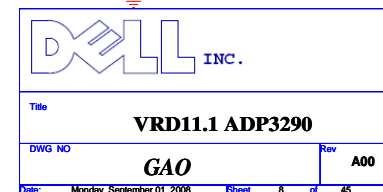
BTX P/S

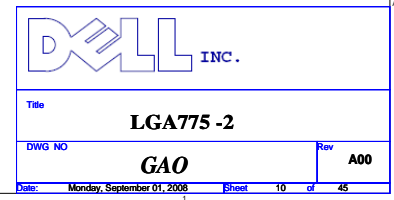












CPUUE 5 OF 7		
AG22	VCCP1	VCCP93
K29	VCCP2	VCCP94
AM26	VCCP3	VCCP95
AE12	VCCP5	VCCP96
AE11	VCCP6	VCCP97
W23	VCCP7	VCCP98
W24	VCCP8	VCCP99
W25	VCCP9	VCCP100
T25	VCCP10	VCCP101
T28	VCCP11	VCCP102
AL18	VCCP12	VCCP103
AC25	VCCP13	VCCP104
W30	VCCP14	VCCP105
V30	VCCP15	VCCP106
AN14	VCCP16	VCCP107
AD28	VCCP17	VCCP108
Y26	VCCP18	VCCP109
AC29	VCCP19	VCCP110
N29	VCCP20	VCCP111
U24	VCCP21	VCCP112
J23	VCCP22	VCCP113
AC27	VCCP23	VCCP114
AM18	VCCP24	VCCP115
AM19	VCCP25	VCCP116
AB8	VCCP26	VCCP117
AC26	VCCP27	VCCP118
J8	VCCP28	VCCP119
T28	VCCP29	VCCP120
T30	VCCP30	VCCP121
AM9	VCCP31	VCCP122
AF16	VCCP32	VCCP123
AC8	VCCP33	VCCP124
AE14	VCCP34	VCCP125
N23	VCCP35	VCCP126
W29	VCCP36	VCCP127
U24	VCCP37	VCCP128
AC24	VCCP38	VCCP129
AC23	VCCP39	VCCP130
Y23	VCCP40	VCCP131
AN26	VCCP41	VCCP132
AN25	VCCP42	VCCP133
AN18	VCCP43	VCCP134
AN11	VCCP44	VCCP135
Y27	VCCP45	VCCP136
Y26	VCCP46	VCCP137
AD24	VCCP47	VCCP138
AE23	VCCP48	VCCP139
AE22	VCCP49	VCCP140
AN19	VCCP50	VCCP141
V8	VCCP51	VCCP142
K9	VCCP52	VCCP143
AE21	VCCP53	VCCP144
AM30	VCCP54	VCCP145
AE19	VCCP55	VCCP146
AC30	VCCP56	VCCP147
AE16	VCCP57	VCCP148
N30	VCCP58	VCCP149
K27	VCCP59	VCCP150
M24	VCCP60	VCCP151
AN21	VCCP61	VCCP152
T8	VCCP62	VCCP153
AC28	VCCP63	VCCP154
N25	VCCP64	VCCP155
W26	VCCP65	VCCP156
AE18	VCCP66	VCCP157
W26	VCCP67	VCCP158
AD25	VCCP68	VCCP159
M8	VCCP69	VCCP160
N30	VCCP70	VCCP161
AD26	VCCP71	VCCP162
A126	VCCP72	VCCP163
AM29	VCCP73	VCCP164
M25	VCCP74	VCCP165
M26	VCCP75	VCCP166
L8	VCCP76	VCCP167
U25	VCCP77	VCCP168
Y8	VCCP78	VCCP169
A112	VCCP79	VCCP170
AD27	VCCP80	VCCP171
U23	VCCP81	VCCP172
M23	VCCP82	VCCP173
AG29	VCCP83	VCCP174
N27	VCCP84	VCCP175
AM22	VCCP85	VCCP176
U28	VCCP86	VCCP177
K28	VCCP87	VCCP178
U8	VCCP88	VCCP179
AK18	VCCP89	VCCP180
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	VCCP93	VCCP184

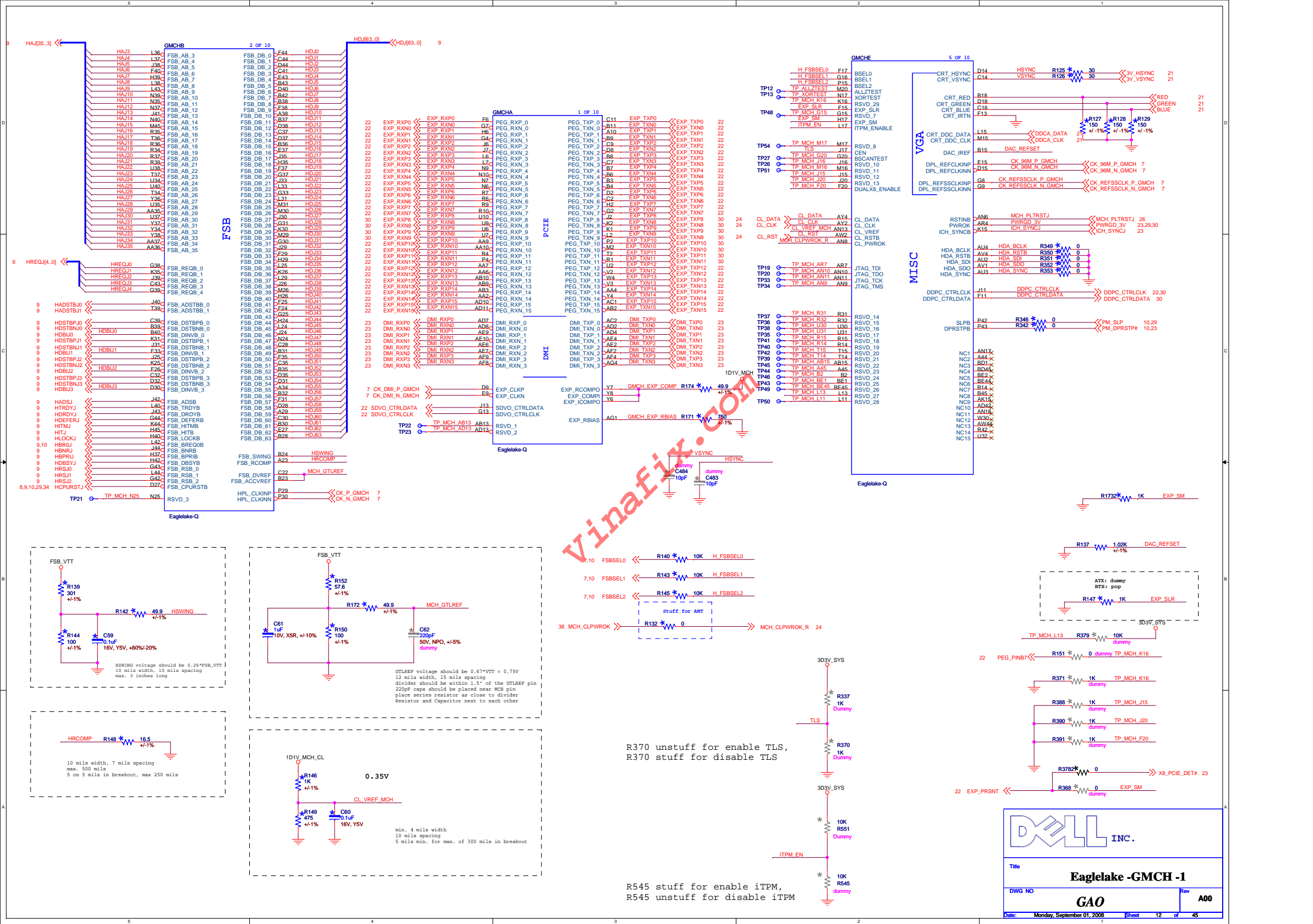
CPU Socket PGA775
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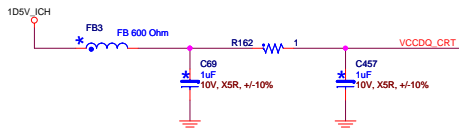
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AF22	VCCP186	VSS42
T29	VCCP187	VSS43
AJ14	VCCP188	VSS44
AM25	VCCP189	VSS45
AH29	VCCP190	VSS46
AH27	VCCP191	VSS47
AG28	VCCP192	VSS48
AK26	VCCP193	VSS49
AM12	VCCP194	VSS50
J27	VCCP195	VSS51
T24	VCCP196	VSS52
T28	VCCP197	VSS53
W28	VCCP198	VSS54
J12	VCCP199	VSS55
U30	VCCP200	VSS56
AG19	VCCP201	VSS57
AL9	VCCP202	VSS58
AD30	VCCP203	VSS59
AF21	VCCP204	VSS60
Y24	VCCP205	VSS61
AK14	VCCP206	VSS62
J9	VCCP207	VSS63
M27	VCCP208	VSS64
J20	VCCP209	VSS65
AF14	VCCP210	VSS66
J30	VCCP211	VSS67
AG18	VCCP212	VSS68
W27	VCCP213	VSS69
AG8	VCCP214	VSS70
AD29	VCCP215	VSS71
AH14	VCCP216	VSS72
W8	VCCP217	VSS73
AH8	VCCP218	VSS74
N24	VCCP219	VSS75
AN22	VCCP220	VSS76
J14	VCCP221	VSS77
AG11	VCCP222	VSS78
AF19	VCCP223	VSS79
N8	VCCP224	VSS80
AF12	VCCP225	VSS81
M28	VCCP226	VSS82
AK9	VCCP227	VSS83
	VCCP228	VSS84
	VCCP229	VSS85
	VCCP230	VSS86
	VCCP231	VSS87
	VCCP232	VSS88
	VCCP233	VSS89
	VCCP234	VSS90
	VCCP235	VSS91
	VCCP236	VSS92
	VCCP237	VSS93
	VCCP238	VSS94
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	VCCP257	VSS113
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	VCCP261	VSS117
	VCCP262	VSS118
	VCCP263	VSS119
	VCCP264	VSS120
	VCCP265	VSS121
	VCCP266	VSS122
	VCCP267	VSS123
	VCCP268	VSS124
	VCCP269	VSS125

CPU Socket PGA775
cpu_lga775h67-1

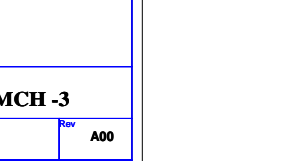
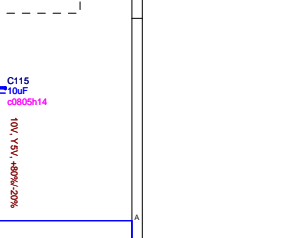
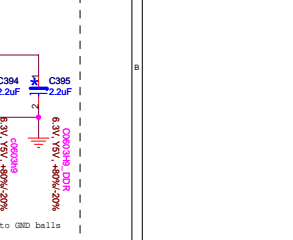
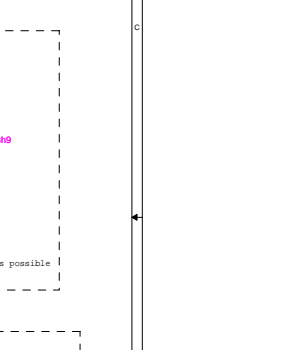
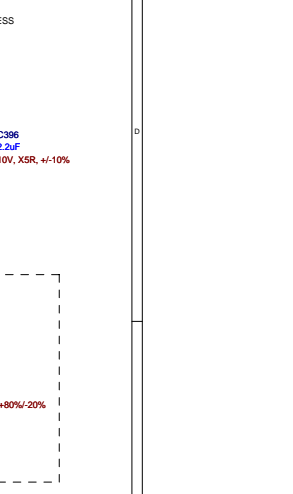
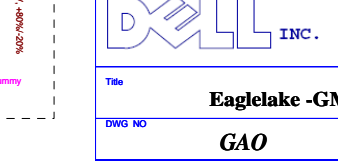
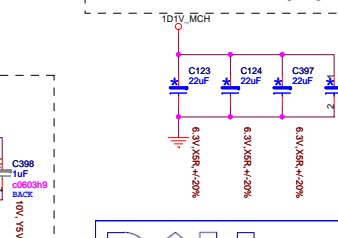
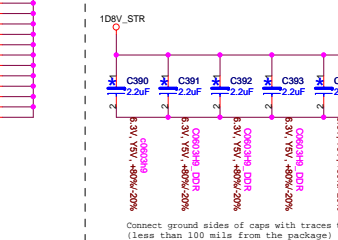
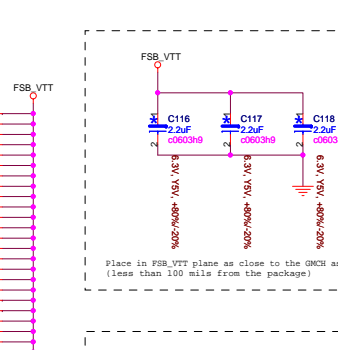
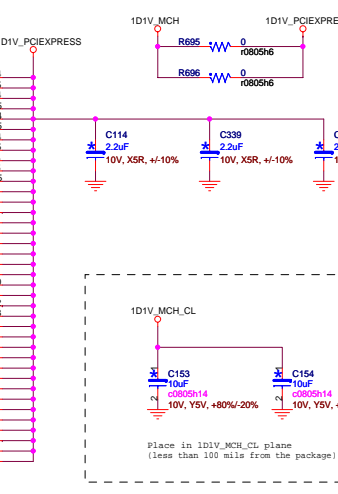
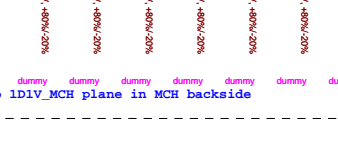
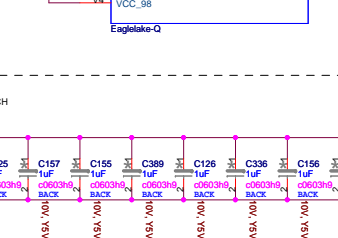
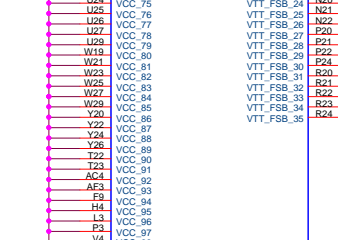
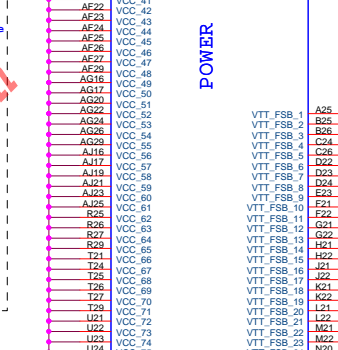
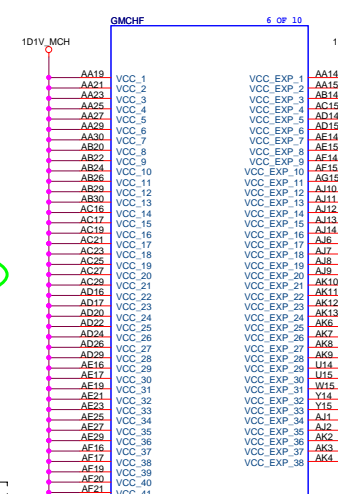
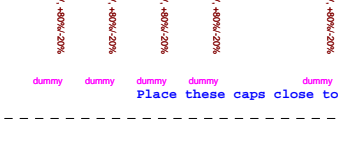
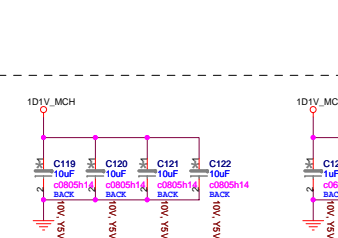
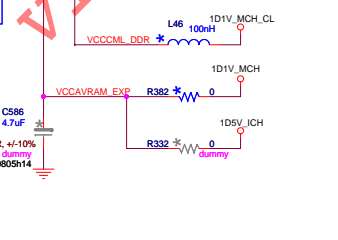
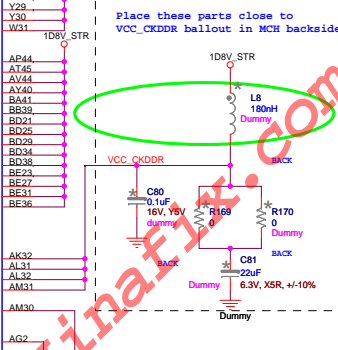
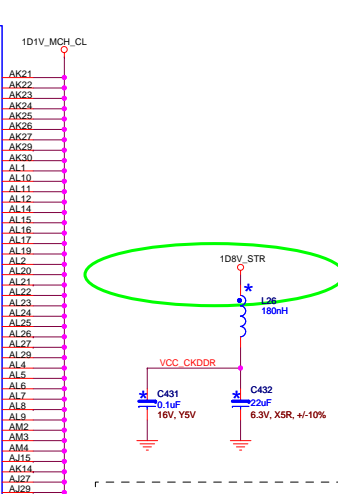
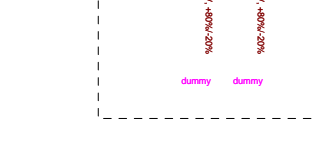
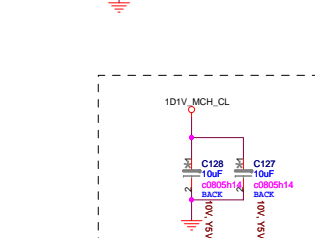
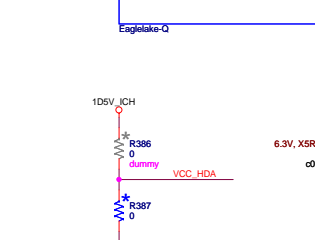
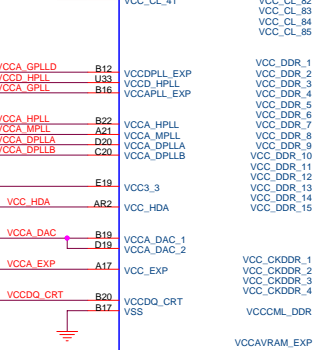
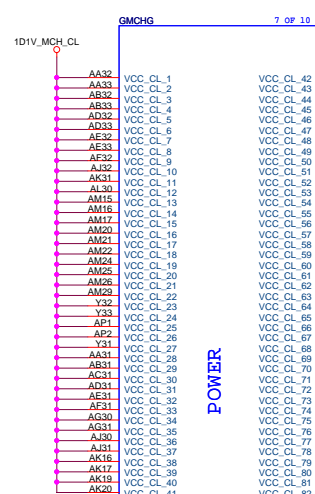
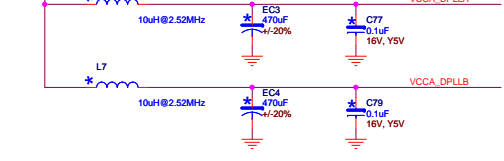
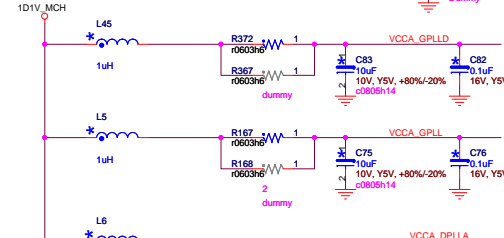
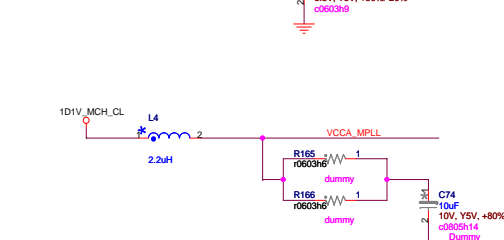
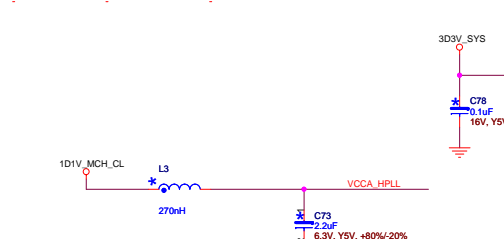
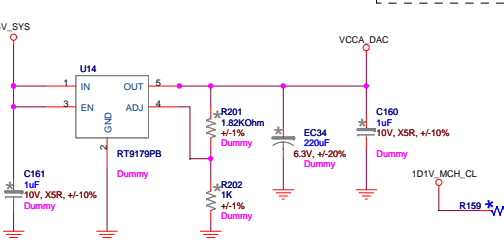
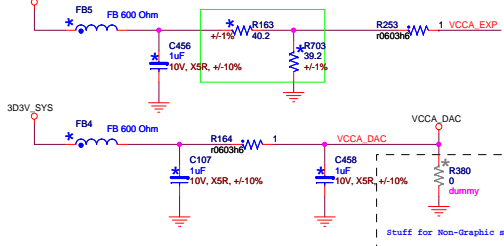
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H22	VSS126	VSS201
H21	VSS127	VSS202
H20	VSS128	VSS203
H19	VSS129	VSS204
H18	VSS130	VSS205
H17	VSS131	VSS206
H16	VSS132	VSS207
H15	VSS133	VSS208
H14	VSS134	VSS209
H13	VSS135	VSS210
H12	VSS136	VSS211
H11	VSS137	VSS212
H10	VSS138	VSS213
H9	VSS139	VSS214
H8	VSS140	VSS215
H7	VSS141	VSS216
H6	VSS142	VSS217
H5	VSS143	VSS218
H4	VSS144	VSS219
H3	VSS145	VSS220
H2	VSS146	VSS221
H1	VSS147	VSS222
	VSS148	VSS223
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	VSS195	VSS270
	VSS196	VSS271
	VSS197	VSS272
	VSS198	VSS273
	VSS199	VSS274
	VSS200	VSS275
	VSS201	VSS276

CPU Socket PGA775
cpu_lga775h67-1





Modify according to Intel MOW50



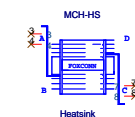
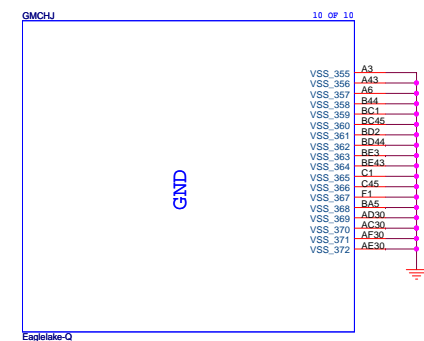
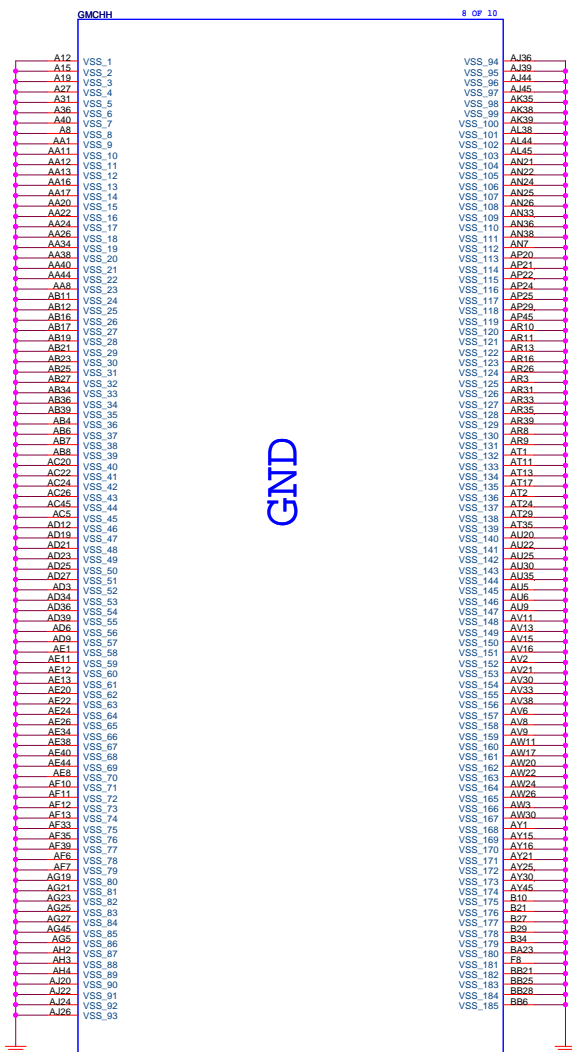
DELL INC.

Eaglelake-GMCH-3

GAB

A00

Monday, September 01, 2008



For GMCH heatsink hook



Title

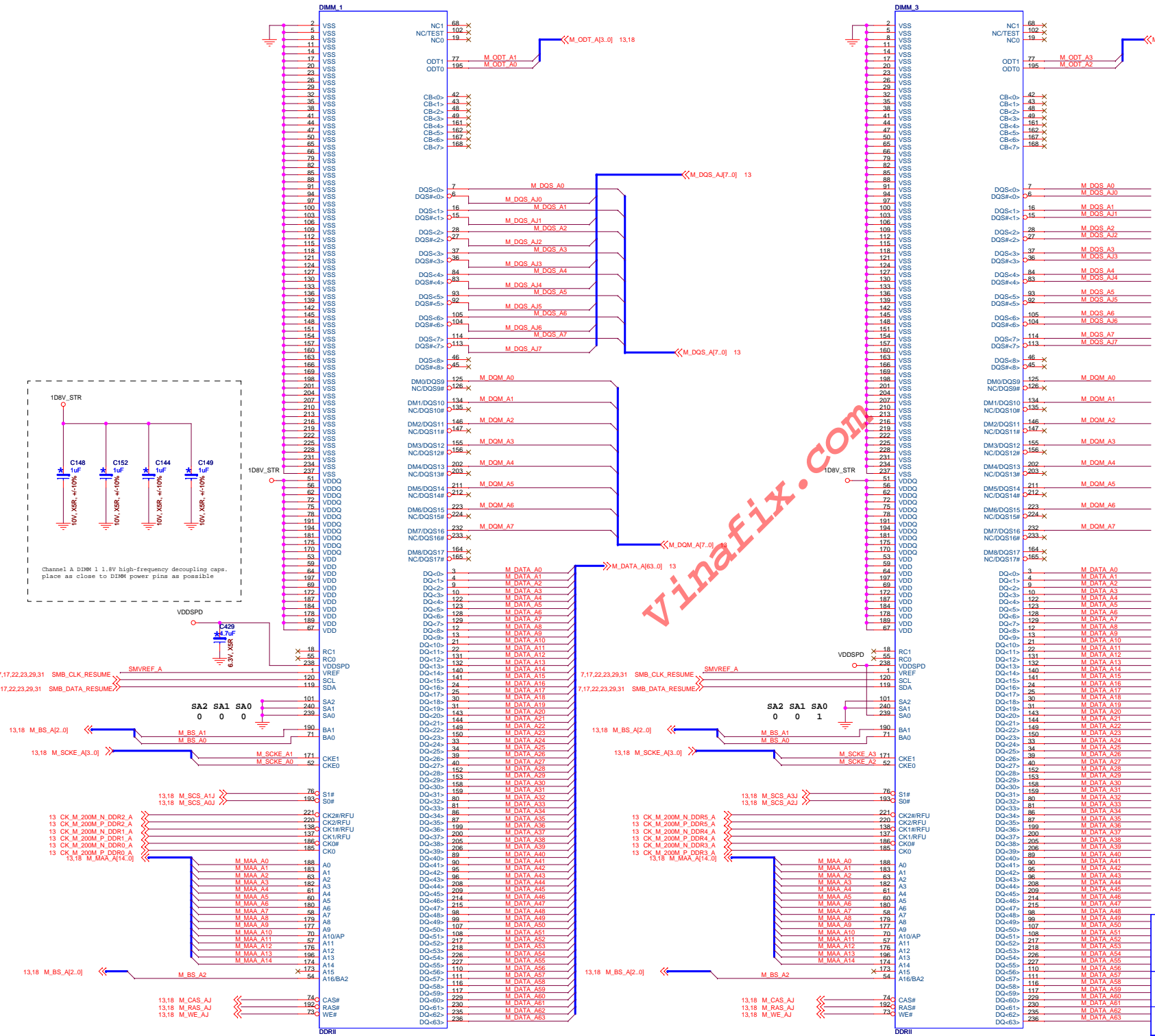
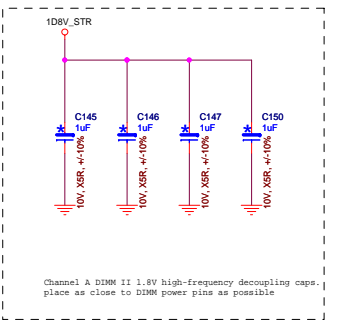
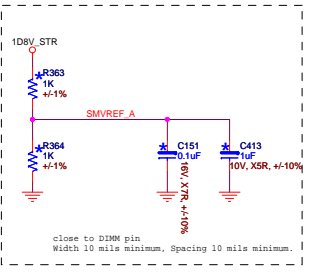
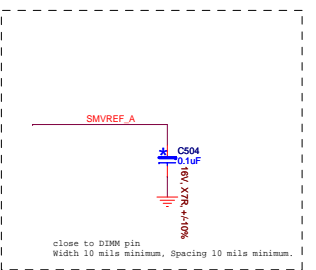
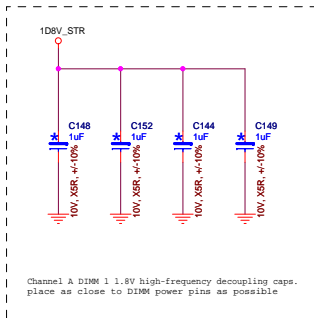
Eaglelake -GMCH -4

DWG NO	
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GAO

Rev	A00
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Date: Monday, September 01, 2008 Sheet 15 of 4





INC.

DDRII Channel A DIMM 1,3

GAO

A00

Rev

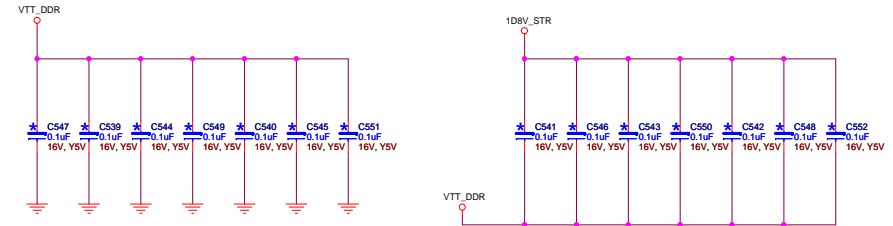
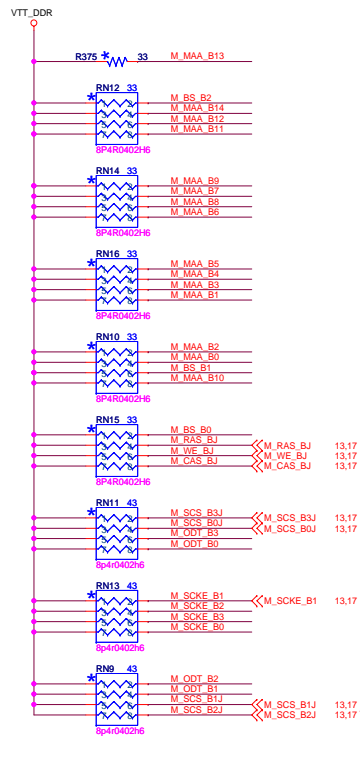
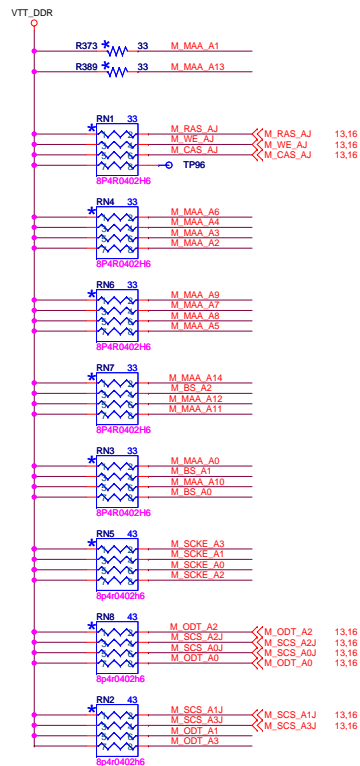
Monday, September 01, 2008

Sheet 16 of 45

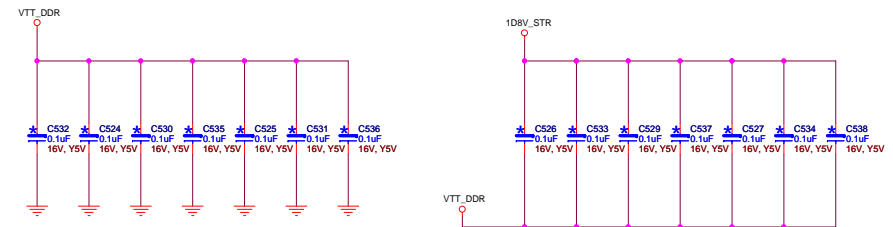


<<M_ODT_A[3..0] 13,16
 <<M_SCKE_A[3..0] 13,16
 <<M_BS_A[2..0] 13,16
 <<M_MAA_A[14..0] 13,16

<<M_SCKE_B[3..0] 13,17
 <<M_BS_B[2..0] 13,17
 <<M_MAA_B[14..0] 13,17
 <<M_ODT_B[3..0] 13,17



Channel A VTT_0.9V high-frequency decoupling caps.
Place as close to termination resistors as possible



Channel B VTT_0.9V high-frequency decoupling caps.
Place as close to termination resistors as possible

23.30 PEG_PINB7_R

12 PEG_PINB7

R2011 8.2K +/-5%

R2004 8.2K +/-5%

Dummy

X16_B4

PEG_PINB81_R

8.2K +/-5%

YS 12V_SYS

SLOT1

B1 12V1

B2 12V2

B3 RSVD8

B4 GND1

B5 SCLK

B6 SMDAT

B7 GND2

B8 3.3V3

B9 JTAG1

B10 3.3V_AUX

B11 WAKE

PRSTN1#

A1

A2

A3

A4

A5 X

A6 X

A7 X

A8 X

A9 X

A10

A11

12V_SYS

3DVS_SYS

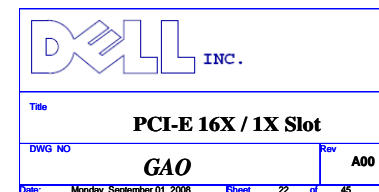
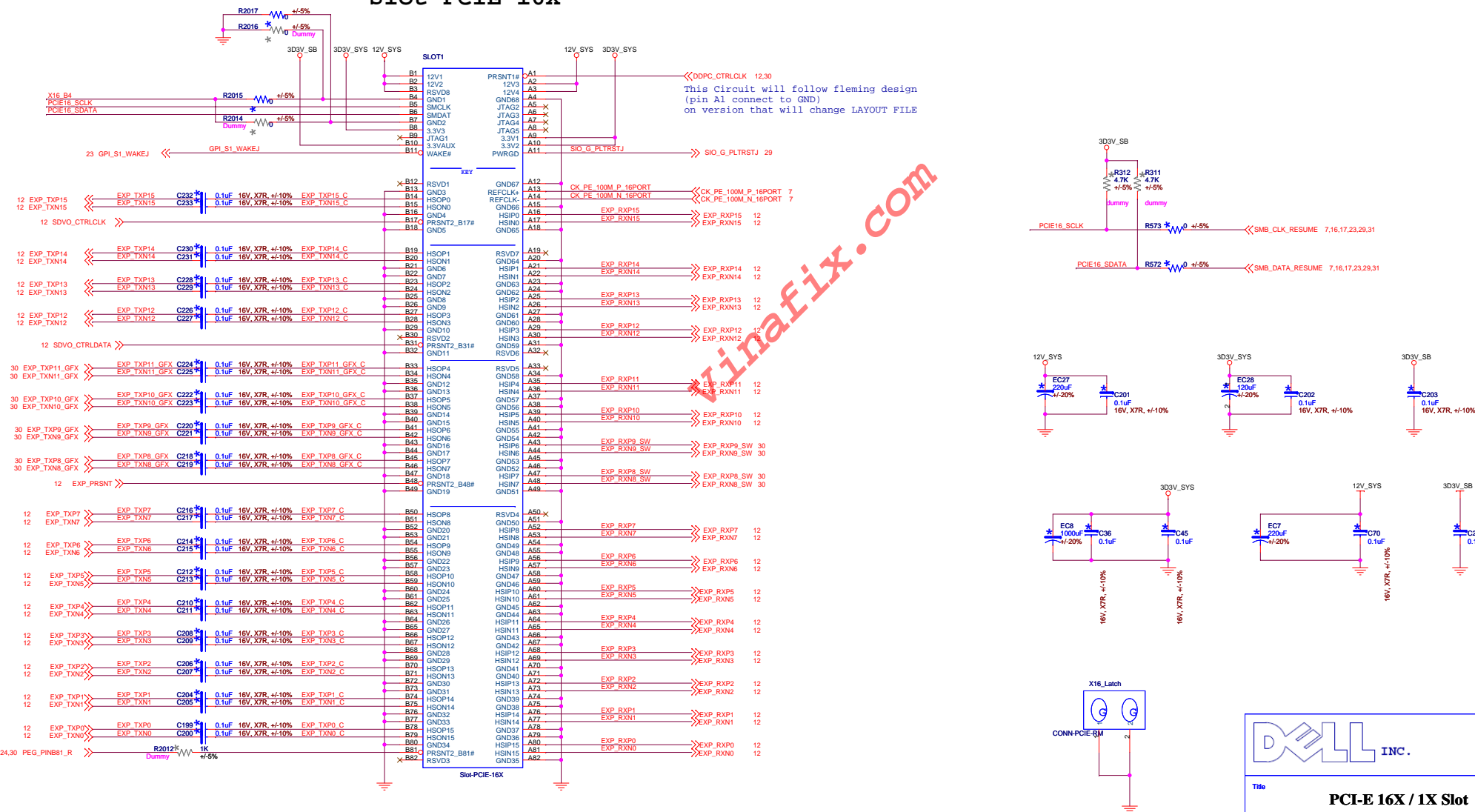
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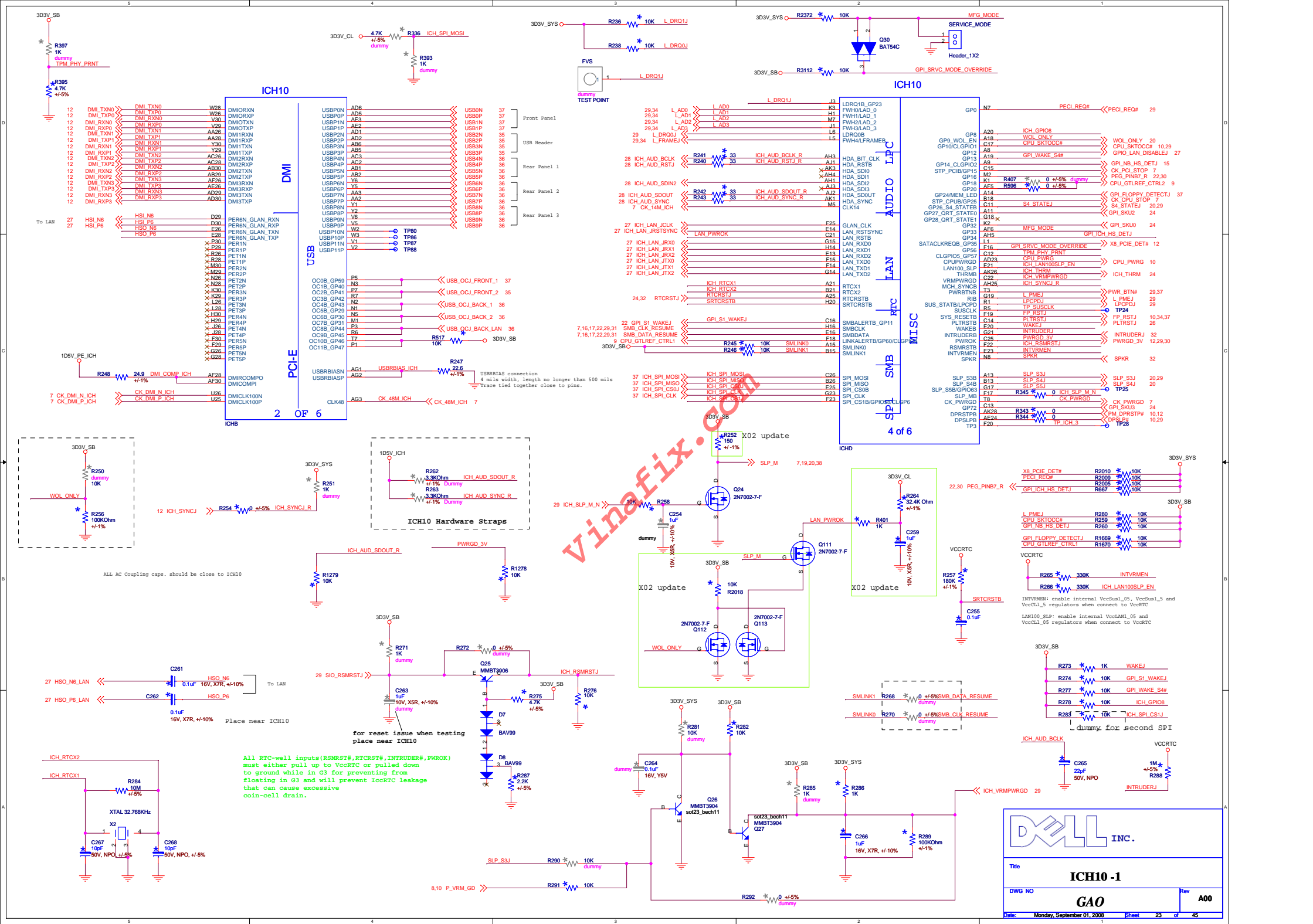
SIO_G_PLTRSTJ

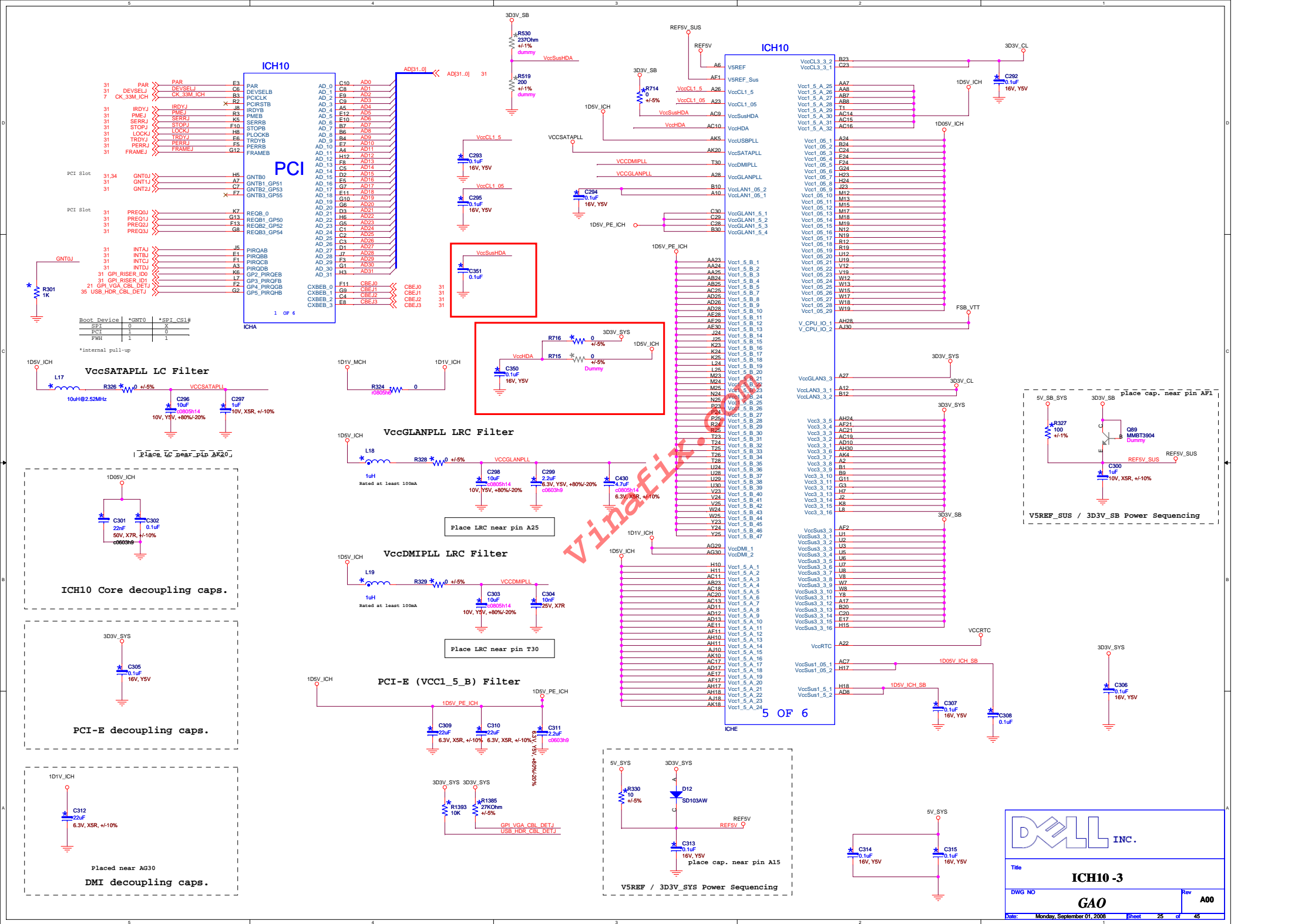
DDPCC_CTRLCLK 12,30

SIO_G_PLTRSTJ 29

This Circuit will follow fleming design (pin A1 connect to GND) on version that will change LAYOUT FILE



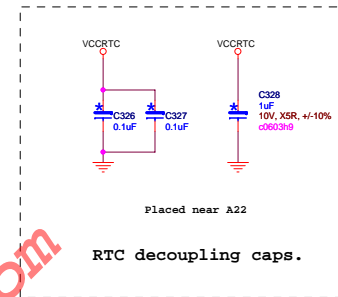
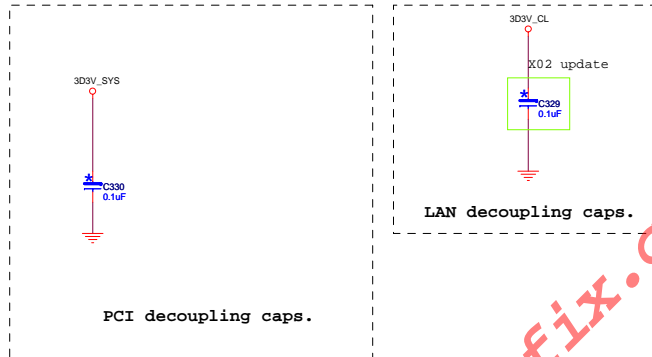
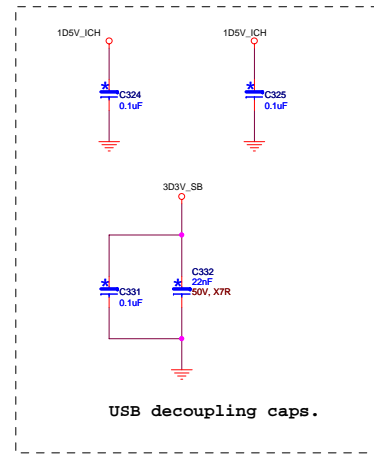
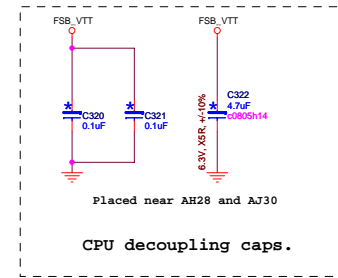
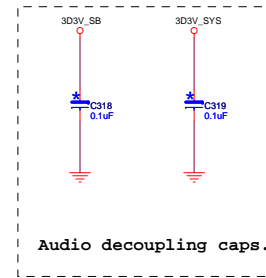
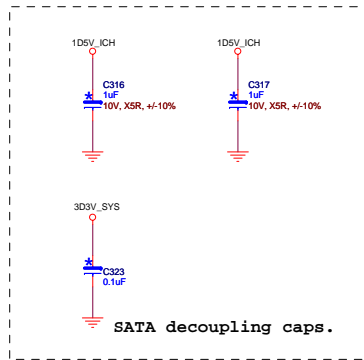




ICH10

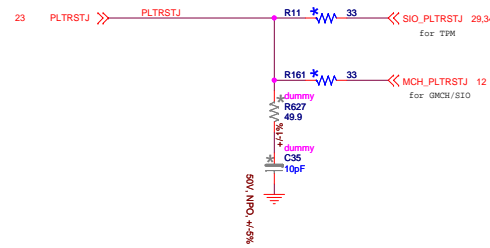
G30	VSS_100	VSS_099	H13
G29	VSS_101	VSS_098	H19
G25	VSS_102	VSS_097	H2
F9	VSS_103	VSS_096	H22
F6	VSS_104	VSS_095	H25
F28	VSS_105	VSS_094	H26
F26	VSS_106	VSS_093	H28
F21	VSS_107	VSS_092	H5
E30	VSS_108	VSS_091	J29
E29	VSS_109	VSS_090	J30
E2	VSS_110	VSS_089	J6
E18	VSS_111	VSS_088	K26
D28	VSS_112	VSS_087	K28
D25	VSS_113	VSS_086	L2
D22	VSS_114	VSS_085	L23
B8	VSS_115	VSS_084	L29
B5	VSS_116	VSS_083	L30
B25	VSS_117	VSS_082	M14
B2	VSS_118	VSS_081	M16
B19	VSS_119	VSS_080	M29
B17	VSS_120	VSS_079	M28
B14	VSS_121	VSS_078	M6
B11	VSS_122	VSS_077	M6
AK9	VSS_123	VSS_076	N13
AK30	VSS_124	VSS_075	N14
AK29	VSS_125	VSS_074	N15
AK2	VSS_126	VSS_073	N16
AK16	VSS_127	VSS_072	N17
AK14	VSS_128	VSS_071	N18
AK12	VSS_129	VSS_070	N23
AJ8	VSS_130	VSS_069	N29
AJ5	VSS_131	VSS_068	N30
AJ23	VSS_132	VSS_067	P12
AJ20	VSS_133	VSS_066	P13
AJ16	VSS_134	VSS_065	P14
AJ14	VSS_135	VSS_064	P15
AH8	VSS_136	VSS_063	P16
AH6	VSS_137	VSS_062	P17
AH2	VSS_138	VSS_061	P18
AH19	VSS_139	VSS_060	P19
AH15	VSS_140	VSS_059	P2
AG28	VSS_141	VSS_058	P28
AF9	VSS_142	VSS_057	P6
AF7	VSS_143	VSS_056	R13
AF29	VSS_144	VSS_055	R14
AF25	VSS_145	VSS_054	R15
AF23	VSS_146	VSS_053	R16
AF20	VSS_147	VSS_052	R17
AF15	VSS_148	VSS_051	R18
AF13	VSS_149	VSS_050	R23
AE9	VSS_150	VSS_049	R29
AE8	VSS_151	VSS_048	R30
AE5	VSS_152	VSS_047	R8
AE26	VSS_153	VSS_046	T12
AE18	VSS_154	VSS_045	T13
AE16	VSS_155	VSS_044	T14
AE15	VSS_156	VSS_043	T15
AE14	VSS_157	VSS_042	T16
AE12	VSS_158	VSS_041	T17
AE10	VSS_159	VSS_040	T18
AE1	VSS_160	VSS_039	T19
AD7	VSS_161	VSS_038	T2
AD3	VSS_162	VSS_037	T29
AD22	VSS_163	VSS_036	T5
AD18	VSS_164	VSS_035	T14
AD16	VSS_165	VSS_034	T15
AD15	VSS_166	VSS_033	T16
AD14	VSS_167	VSS_032	T17
AC8	VSS_168	VSS_031	T18
AC6	VSS_169	VSS_030	T19
AC5	VSS_170	VSS_029	U23
AC30	VSS_171	VSS_028	V13
AC29	VSS_172	VSS_027	V14
AC24	VSS_173	VSS_026	V15
AC12	VSS_174	VSS_025	V16
AC1	VSS_175	VSS_024	V17
AB3	VSS_176	VSS_023	V18
AB28	VSS_177	VSS_022	V26
AB26	VSS_178	VSS_021	V28
AA6	VSS_179	VSS_020	V3
AA5	VSS_180	VSS_019	V7
AK27	VSS_181	VSS_018	W1
AK20	VSS_182	VSS_017	W14
AJ4	VSS_183	VSS_016	W16
AF3	VSS_184	VSS_015	W23
B27	VSS_185	VSS_014	W29
	VSS_186	VSS_013	W30
	VSS_187	VSS_012	W6
	VSS_188	VSS_011	Y26
	VSS_189	VSS_010	Y3
	VSS_190	VSS_009	Y7
	VSS_191	VSS_008	AA30
	VSS_192	VSS_007	AA29
	VSS_193	VSS_006	AA1
		VSS_005	A30
		VSS_004	A1
		VSS_003	
		VSS_002	
		VSS_001	

ICH10 6 OF 6

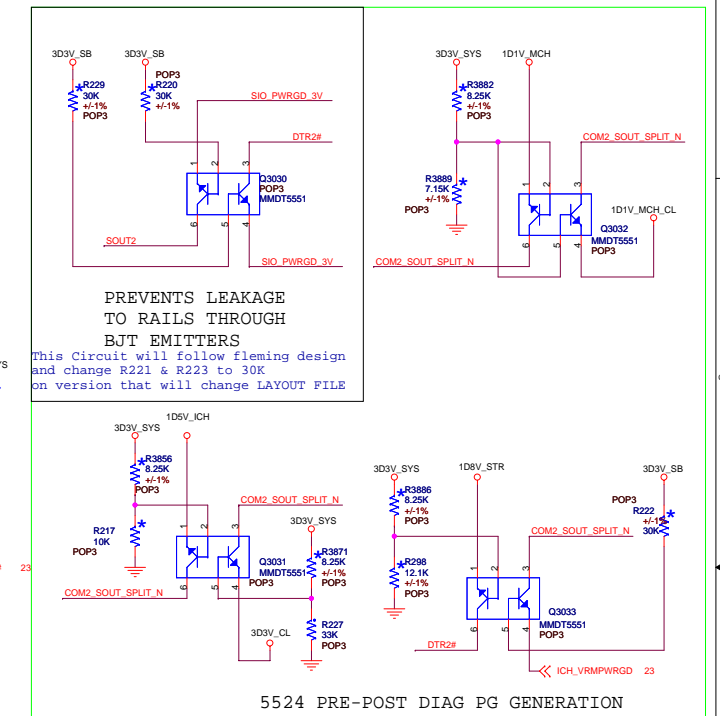
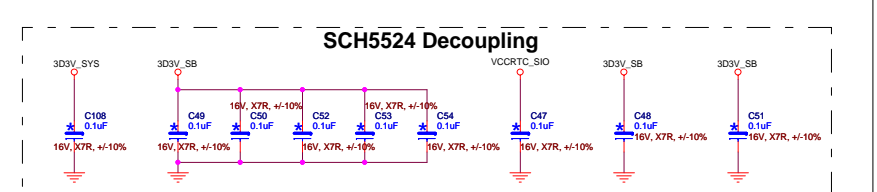
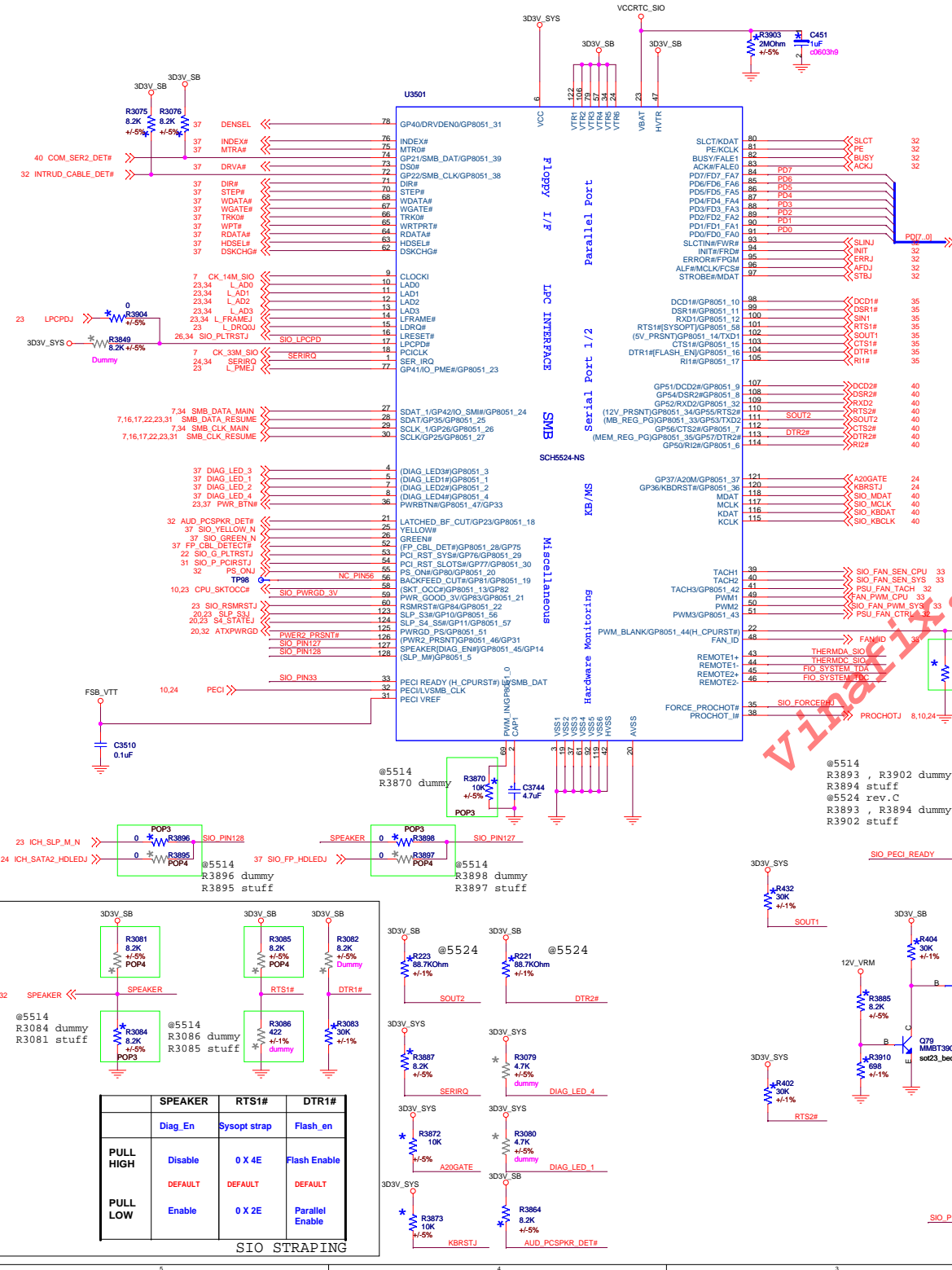


PCI decoupling caps.

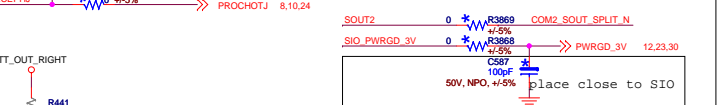
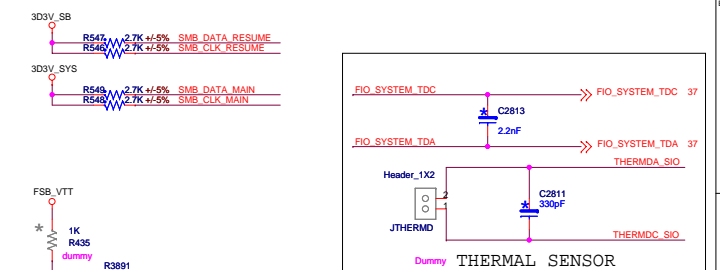
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DELL INC.	
Title ICH10 -4	
DWG NO GAO	Rev A00
Date: Monday, September 01, 2008	Sheet 26 of 45



5524 PRE-POST DIAG PG GENERATION



Super I/O--SMSC5524/5514E

GAO

A00

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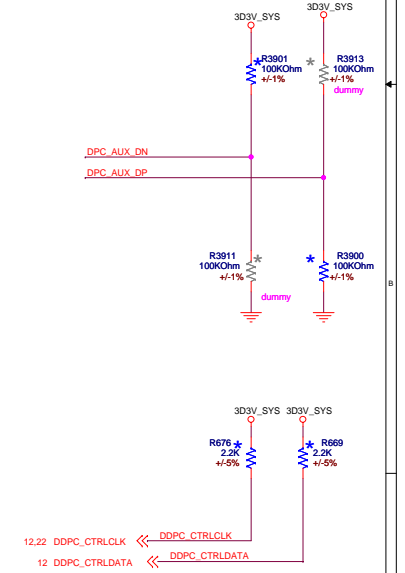
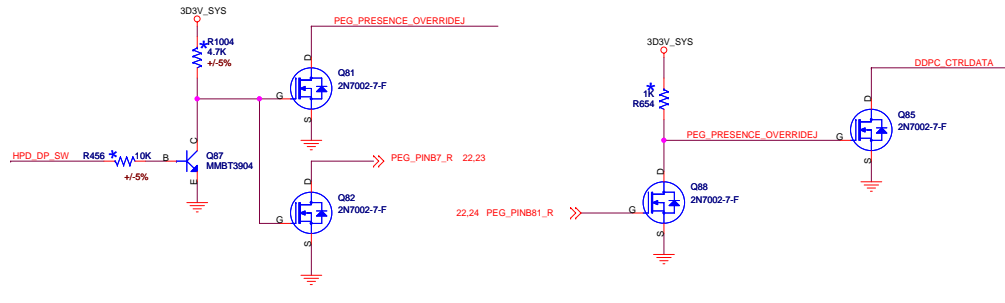
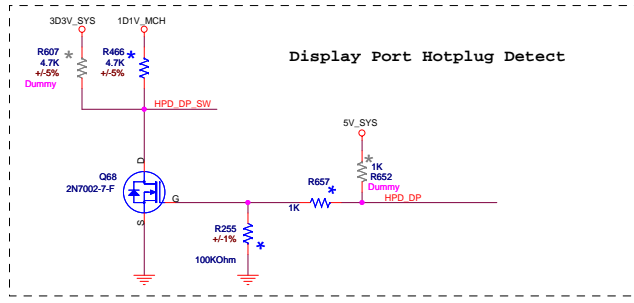
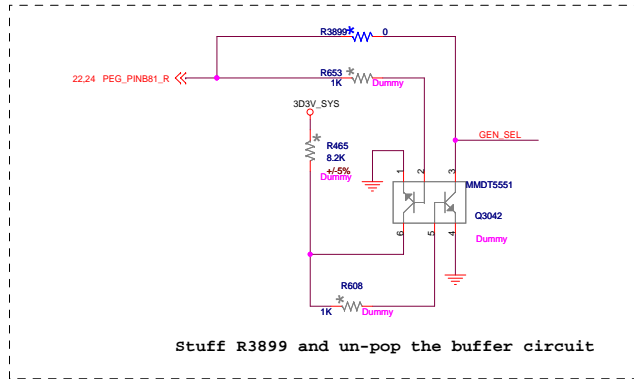
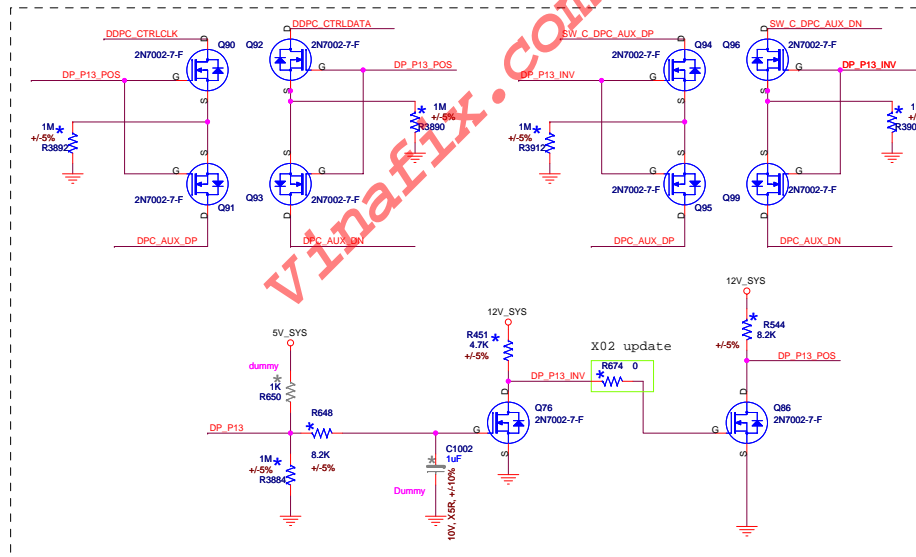
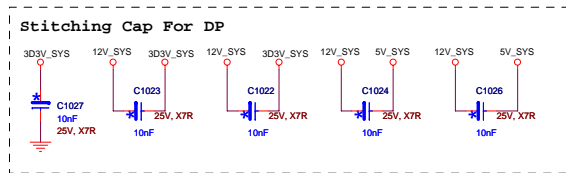
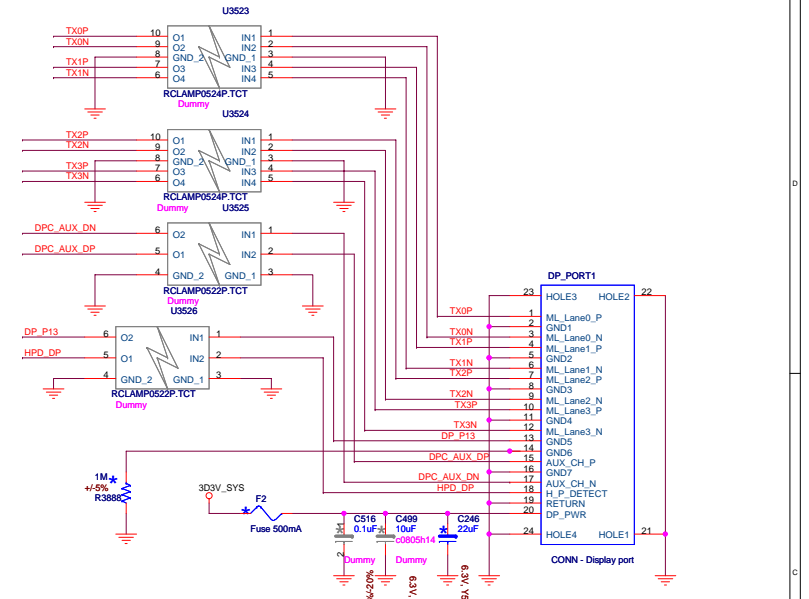
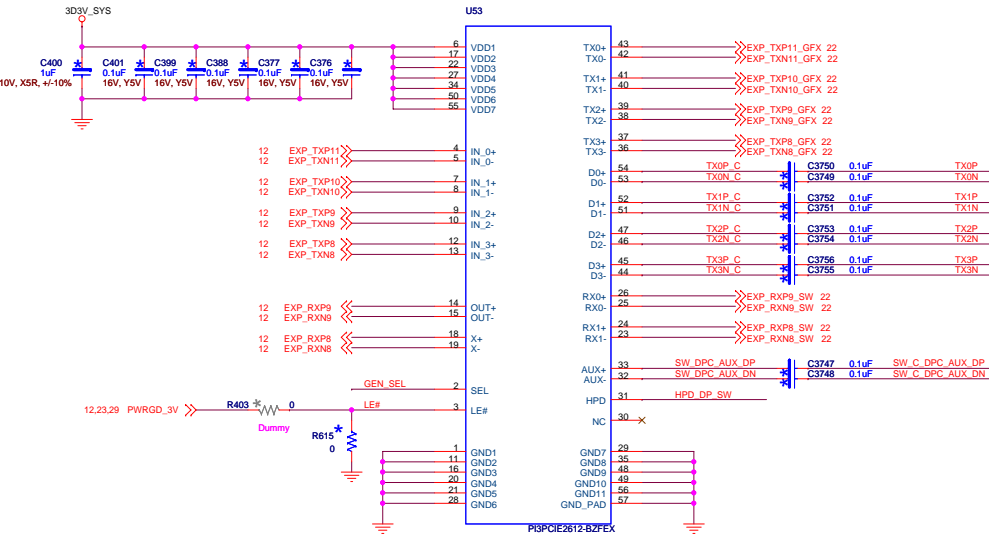
Sheet 29 of 45

	SPEAKER	RTS1#	DTR1#
	Diag_En	Sysopt strap	Flash_en
PULL HIGH	Disable	0 X 4E	Flash Enable
DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	Enable	0 X 2E	Parallel Enable

SIO STRAPPING

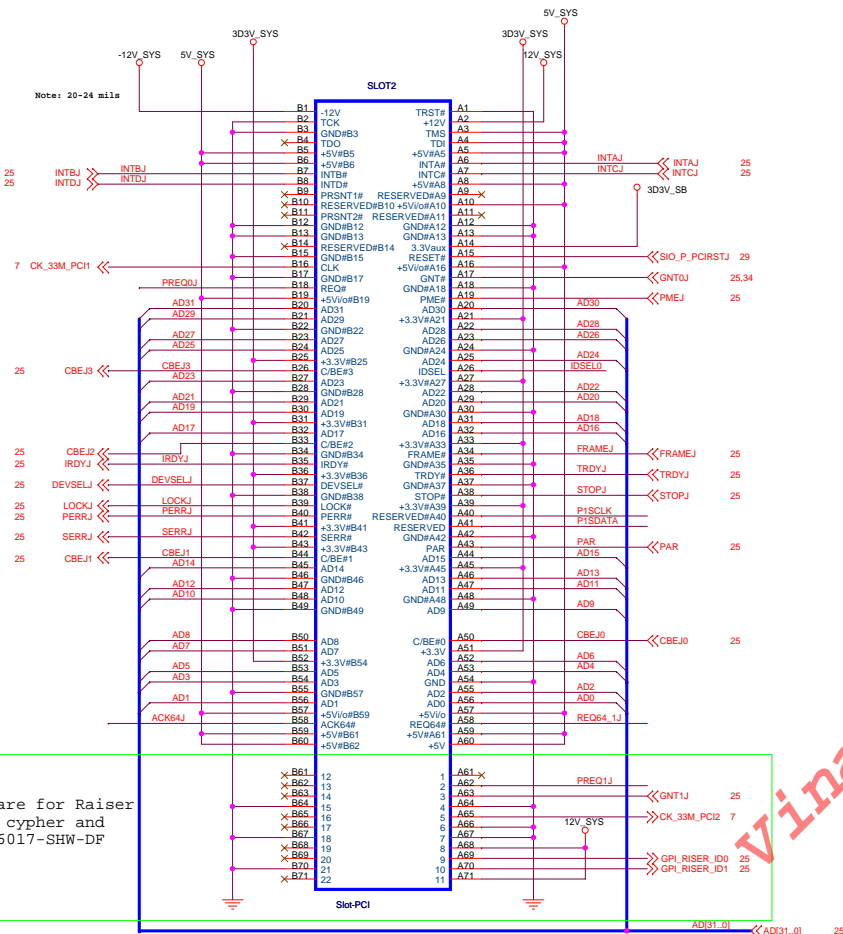
GENII SWITCH

DISPLAY PORT

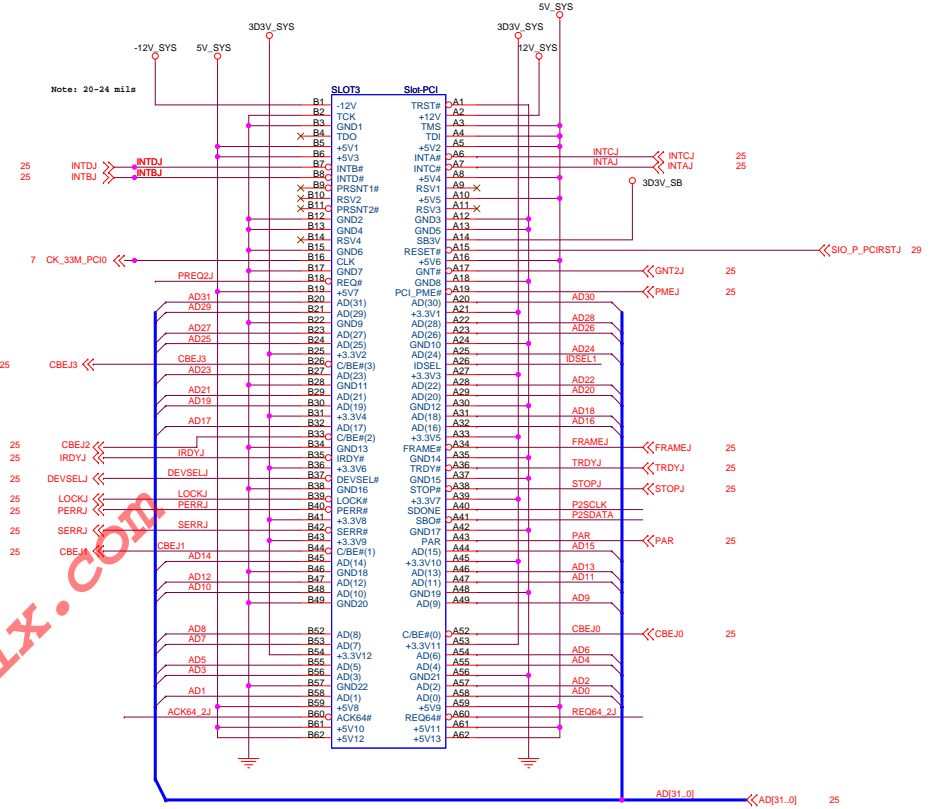


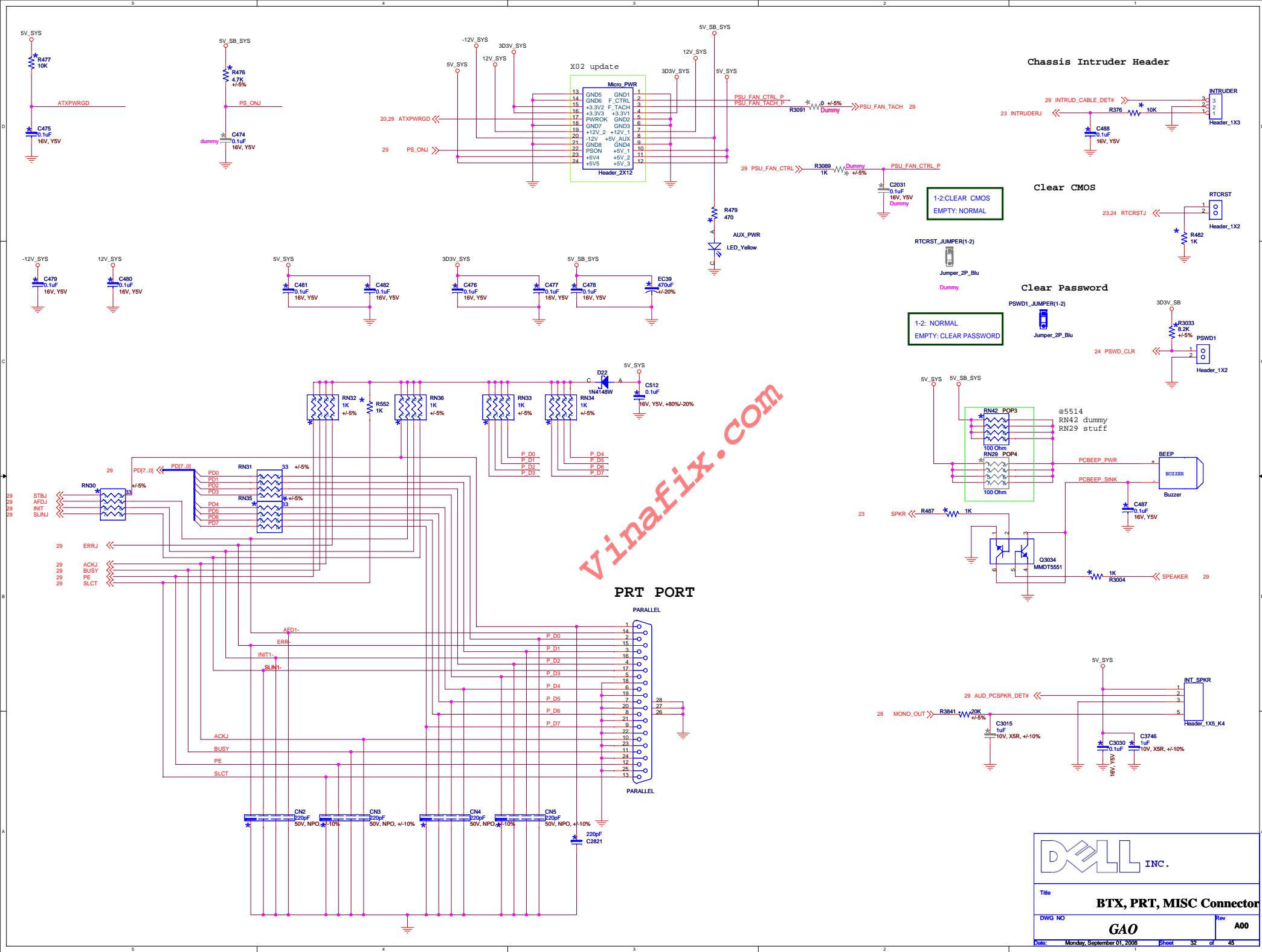
Title	
GenII Switch / DP	
DWG NO	Rev
GAO	A00
Date	Monday, September 01, 2008
Sheet	30 of 45

PCI SLOT W/ RISER ONLY FOR NEO
PCI SLOT W/O RISER FOR SMITH & CYPHER



PCI-SLOT3 DUMMY FOR CYPHER






Chassis Intruder Header

Clear CMOS

Clear Password

PRT PORT



INC.

Title

BTX, PRT, MISC Connector

DWG NO

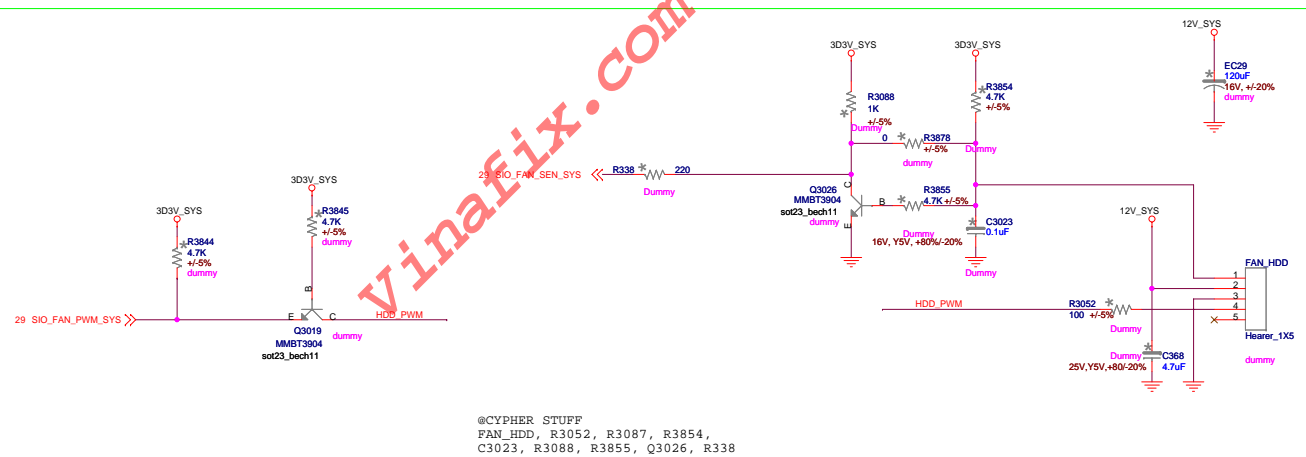
GAO

Rev

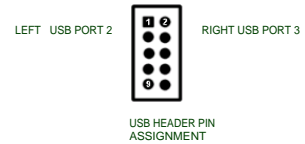
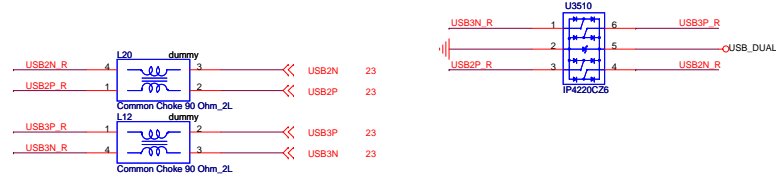
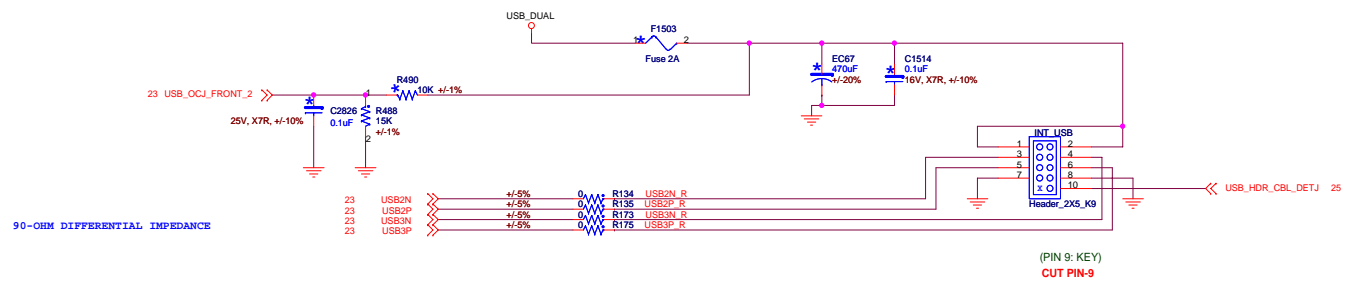
A00

Date: Monday, September 01, 2008

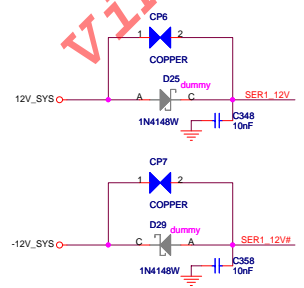
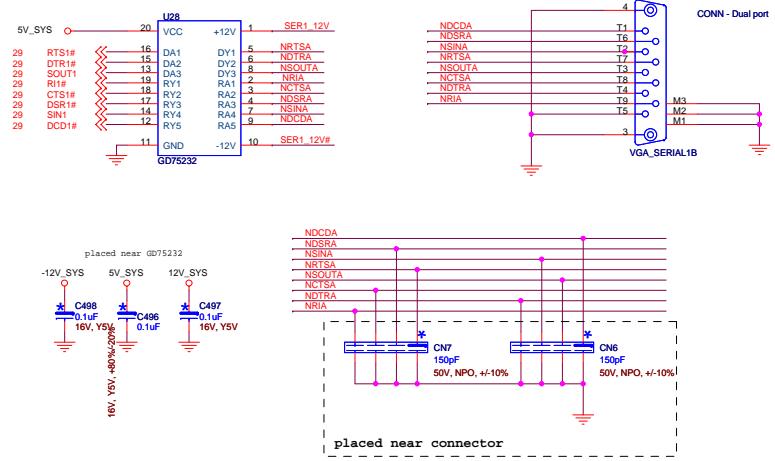
Sheet 32 of 45



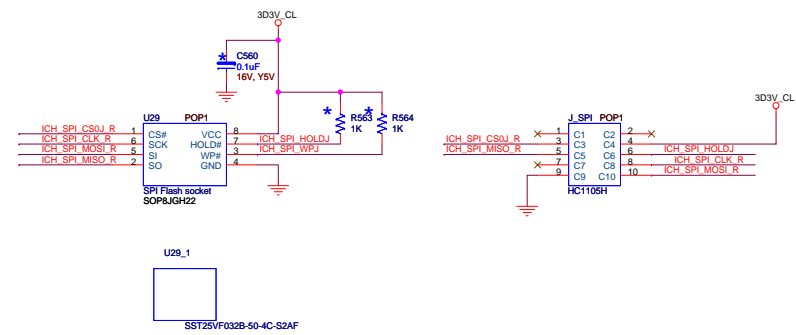
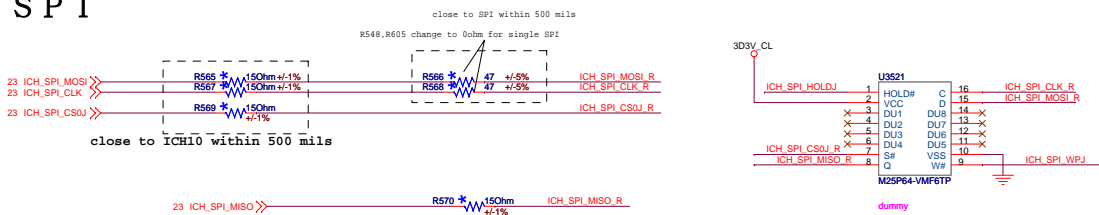
USB



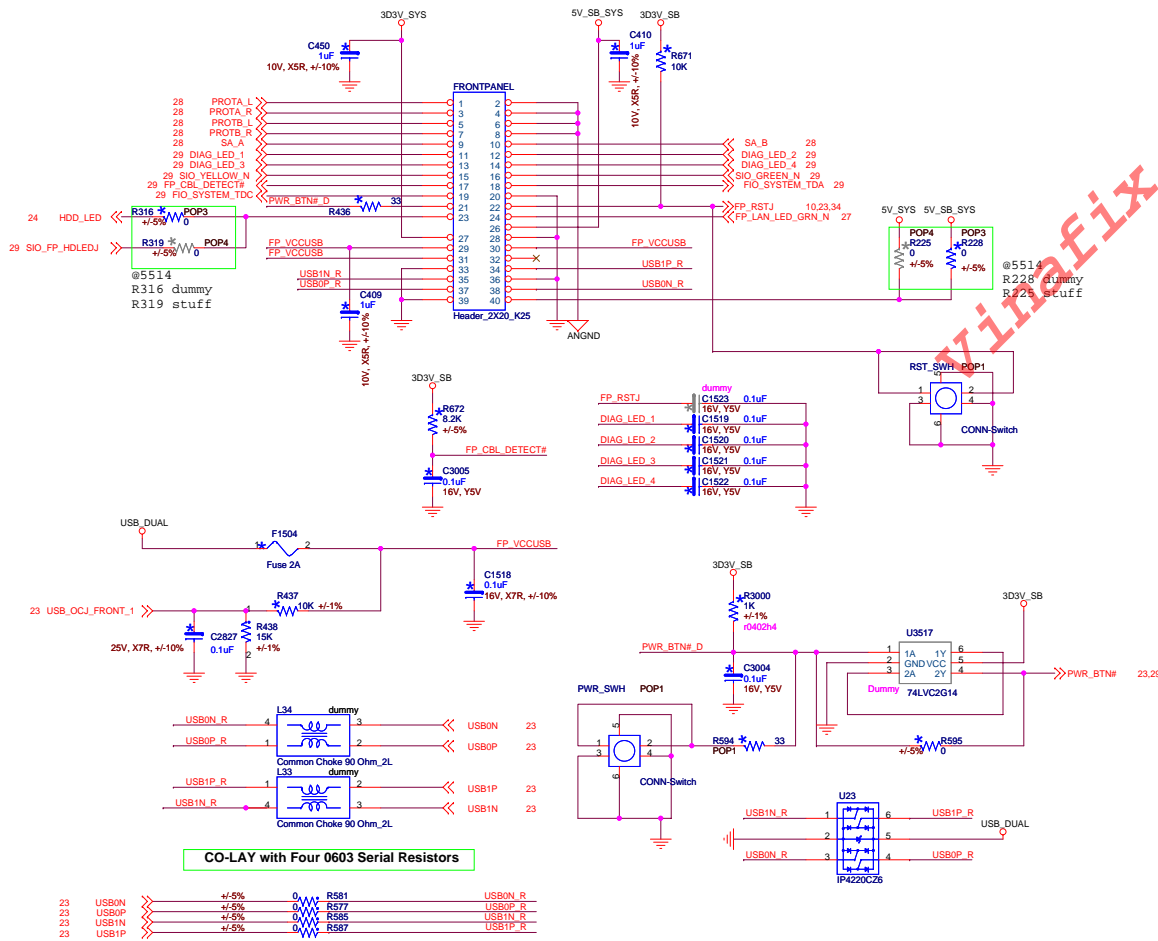
COM 1



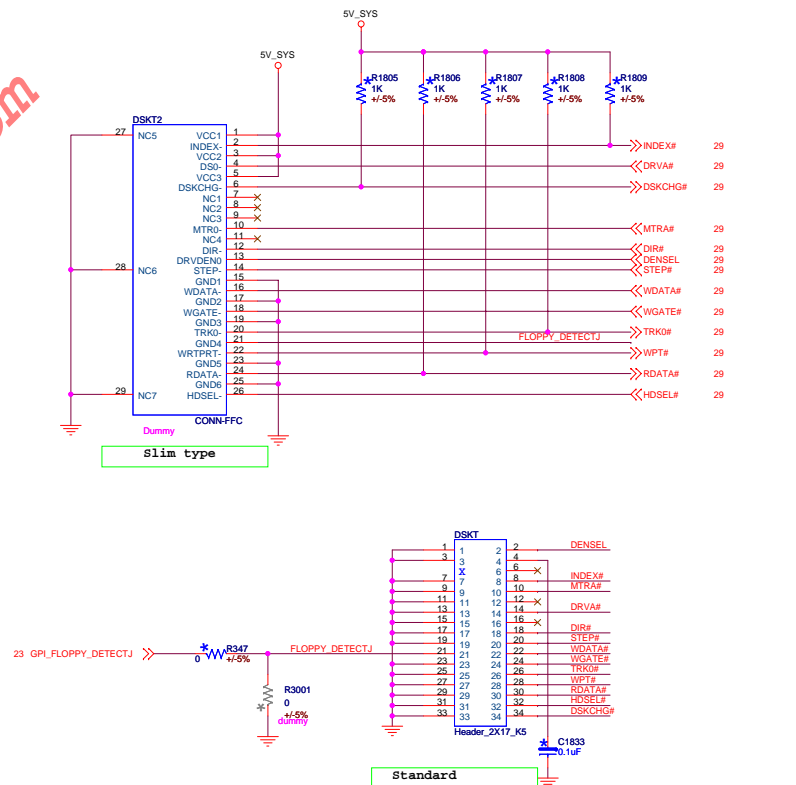
S P I



FRONT PANEL



FLOPPY



Title **Front Panel / SPI / Floppy**

GAO

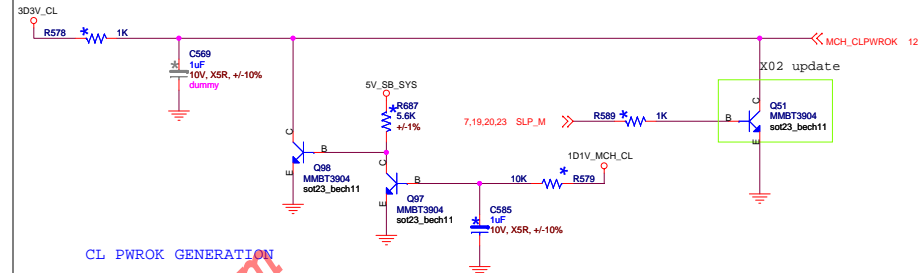
A00

Stuff for AMT

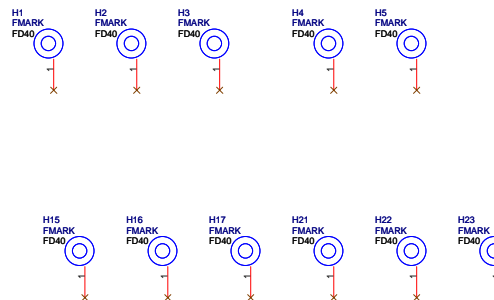
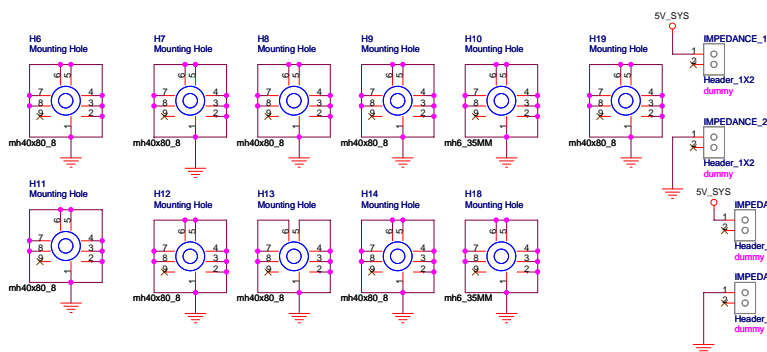
The diagram illustrates the electrical connections for the AMT (Active Management Technology) controller, specifically the Q51 MM68T3904. Key components and connections include:

- Power Supply:** A 3D3V_CL input is connected to a 1K resistor (R578) and a 10V, 5% capacitor (C569) to ground. A 5V_SB_SYS supply is connected to a 5.6K resistor (R687) and a 10V, 5% capacitor (C585) to ground.
- Signal Connections:** The Q51 controller's pins are connected to MCH_CLPWROK and X02 update signals. The controller is also connected to a 10K resistor (R589) and a 10V, 5% capacitor (C579) to ground.
- Transistors:** Two NPN transistors, Q56 and Q57 (MM68T3904), are shown. Q56 is connected to the 5V_SB_SYS supply and the 10V, 5% capacitor (C585). Q57 is connected to the 10V, 5% capacitor (C585) and the 10K resistor (R589).
- Other Components:** A 1D1V_MCH_CL signal is connected to the controller's pins. A 10K resistor (R579) is connected to the controller's pins and ground.

CL PWROK GENERATION



CL PWROK GENERATION



Title

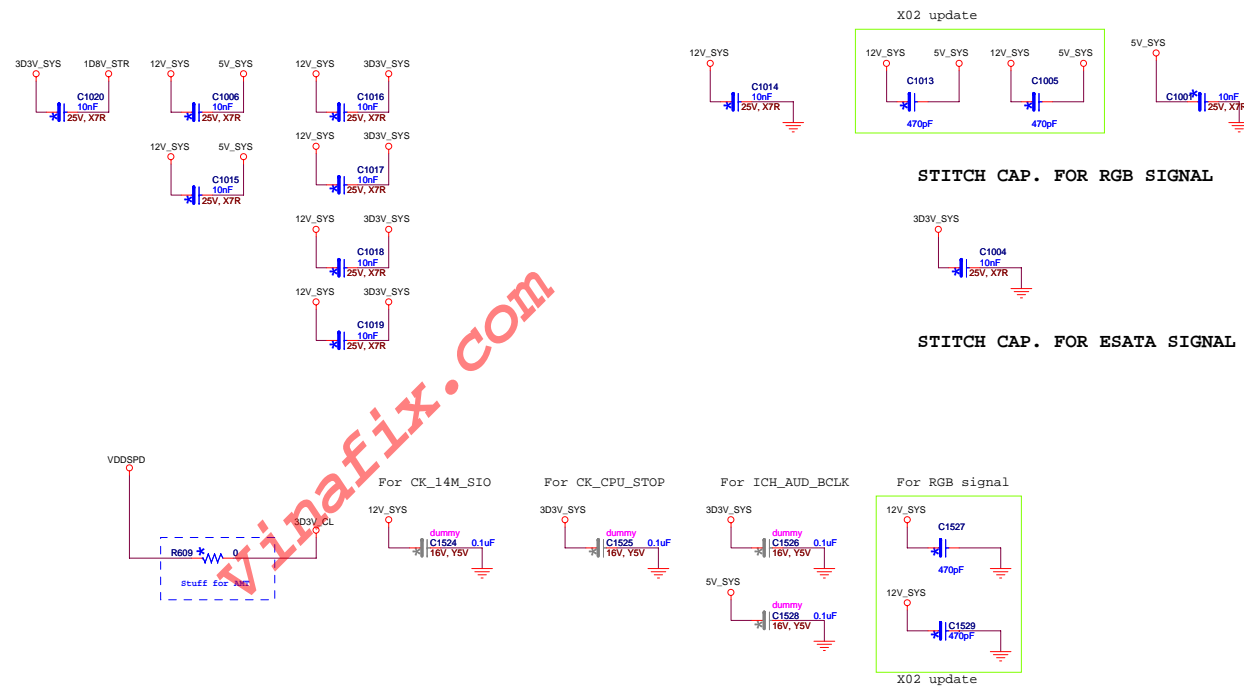
Reserved-1

DWG NO	
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GAO

Rev	A00
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Title

Reserved-2

DWG NO	
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GAO

Rev	A00
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5	4	3	2	1
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PCI Routing Summary

	PCI0	PCI1				
INTAJ	A	C				
INTBJ	B	D				
INTCJ	C	A				
INTDJ	D	B				
INTEJ						
INTFJ						
INTGJ						
INTHJ						

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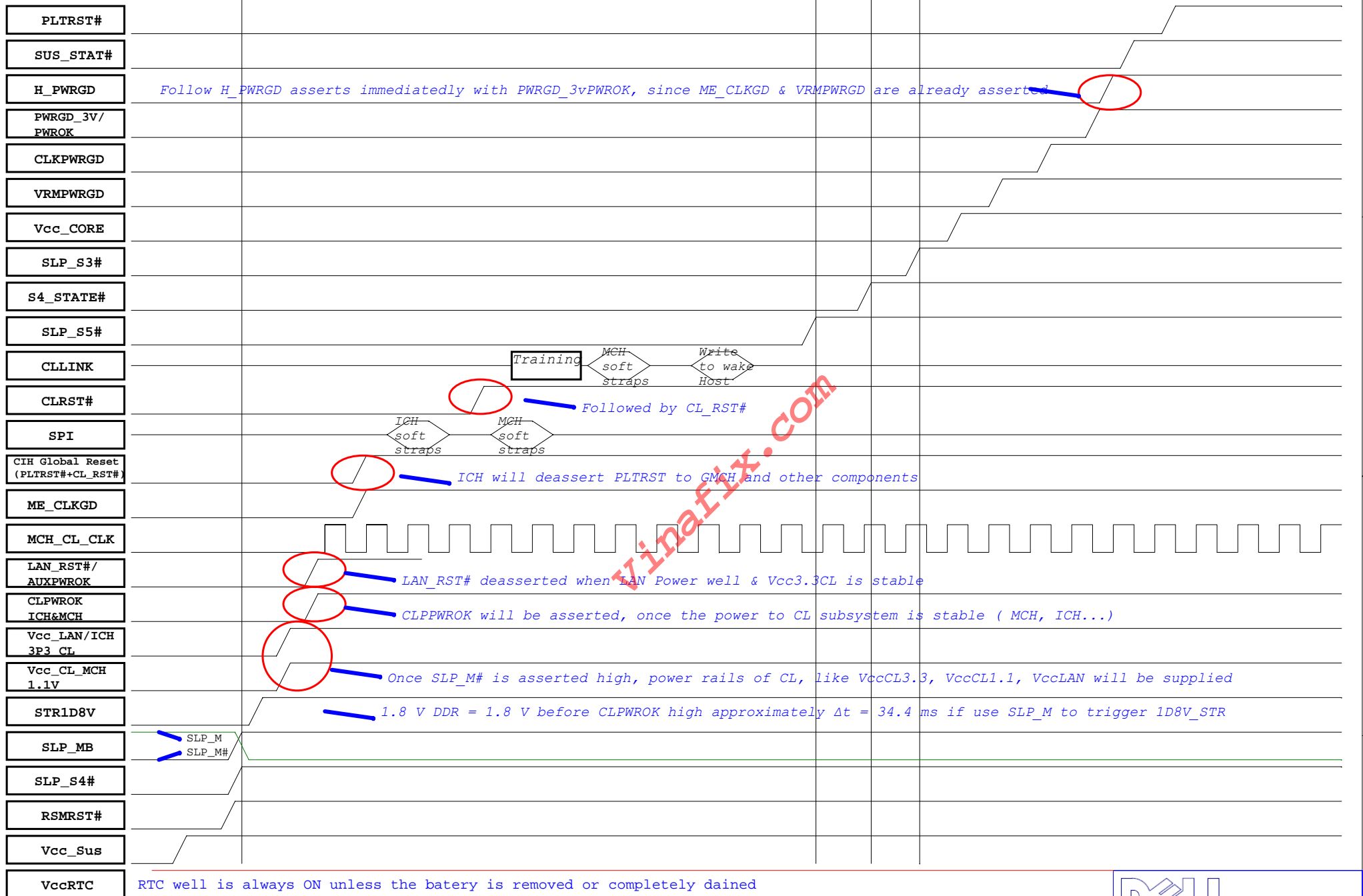
G3/M-OFF

S5/M1

S4/M1

S3/M1

S0/M0

Title
AMT TIMINGDWG NO
GAORev
A00

Date: Monday, September 01, 2008 Sheet 43 of 45

Clock Gen IDTCV184 Functional Straps

PIN NAME	NET		Strapping description
PCI2/TME (PIN4)	CK_PIN4	1	Overclocking DISABLED DEFAULT
		0	Overclocking ENABLED
PCI3/CPGP (PIN5)	CK_PIN5	1	CGP TABLE ENABLED
		0	CGP TABLE DISABLED DEFAULT
PCI4/SRC5_EN (PIN6)	CK_PIN6	1	SRC5
		0	CPU_STOP# and PCI_STOP# DEFAULT
PCI_F5/ITP_EN (PIN7)	CK_PIN7	1	CPU_ITP DEFAULT
		0	SRC8

SIO SMSC5524 Functional Straps

PIN NAME	NET		Strapping description
SPEAKER[DIAG_EN#] /GP8051_45/GPI4 (PIN127)	SPEAKER	1	Diag.En Disable
		0	Diag.En Enable DEFAULT
RTS1#[SYSOPT] /GP8051_58 (PIN101)	RTS1#	1	Sysopt strap 0 X 4E
		0	Sysopt strap 0 X 2E
DTR1#[FLASH_EN] /GP8051_16 (PIN104)	DTR1#	1	Flash Enable
		0	Parallel Enable DEFAULT

Intel ICH10 Functional Straps

PIN NAME	NET		Strapping description
TP3	TP68	1	Danbury Technology Enable Internal Pull-up
		0	XOR Chain Entrance
SPKR	SPKR	1	NoReboot mode Internal Pull-up
		0	Reboot mode
GPIO33 / HDA_DOCK_EN#	MFG_MODE	1	MEEnable DEFAULT
		0	ME disable
SPI_MOSI	ICH_SPI_MOSI	1	MCH TPM Enable
		0	MCH TPM disable DEFAULT

Intel MCH Eaglelake Q43 Functional Straps

PIN NAME	NET		Strapping description
cen	TLS	1	TLS Enable
		0	TLS disable
iTPMb	ITPM_EN	1	iTPM Enable
		0	iTPM disable
DDPC_CTRLDATA	DDPC_CTRLDATA	1	SELECT Display Port
		0	SELECT PCIEX16
DDPC_CTRLCLK	DDPC_CTRLCLK	1	SELECT Display Port
		0	SELECT PCIEX16

Chassis	SKU	TPM	TCM	R543	TPM SKU ID					Board ID		
					SKU3	SKU2	SKU1	SKU0	Pop option	REV1	REV0	Pop option
Smith	1	V	X	Stuffed	0	0	0	0	Stuff R2577, R2582, R2013, R2335	0	0	stuff R2001, R2334
Smith	2	X	X	Stuffed	0	0	1	0	Stuff R2313, R2577, R2013, R2335	0	0	stuff R2001, R2334
Smith	3	X	V	Stuffed	0	0	0	1	Stuff R2576, R2582, R2013, R2335	1	1	stuff R2324, R3334
Neo	4	V	X	Stuffed	0	0	0	0	Stuff R2577, R2582, R2013, R2335	0	0	stuff R2001, R2334
Neo	5	X	X	Stuffed	0	0	1	0	Stuff R2313, R2577, R2013, R2335	0	0	stuff R2001, R2334
Neo	6	X	V	Stuffed	0	0	0	1	Stuff R2576, R2582, R2013, R2335	1	1	stuff R2324, R3334
Cypher	7	V	X	Stuffed	0	0	0	0	Stuff R2577, R2582, R2013, R2335	0	0	stuff R2001, R2334
Cypher	8	X	X	Stuffed	0	0	1	0	Stuff R2313, R2577, R2013, R2335	0	0	stuff R2001, R2334
Cypher	9	X	V	Stuffed	0	0	0	1	Stuff R2576, R2582, R2013, R2335	1	1	stuff R2324, R3334

Chassis	Chassis ID			
	ID2	ID1	ID0	Pop option
Smith	0	1	0	Stuff R2346, R418, R2349
Smith	0	1	0	Stuff R2346, R418, R2349
Smith	0	1	0	Stuff R2346, R418, R2349
Neo	0	0	1	Stuff R396, R2347, R2349
Neo	0	0	1	Stuff R396, R2347, R2349
Neo	0	0	1	Stuff R396, R2347, R2349
Cypher	0	0	0	Stuff R2346,R2347, R2349
Cypher	0	0	0	Stuff R2346,R2347, R2349
Cypher	0	0	0	Stuff R2346,R2347, R2349



				
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